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Comparison of Three Buck Topologies for Wide Output Voltage Applications

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***Abstract*—This paper investigates the suitability of three step-down dc-dc converter topologies as the final conversion stage in a wide output voltage modular ac-dc power supply. Single-phase, two-phase and three-level buck converters are evaluated over a wide range of outputs using analytical models and physical measurements. The converters' performance is evaluated at all operating points using statistical analysis of the converter component losses produced to assess their suitability for wide output voltage applications. The dynamic performance of the converters is also evaluated to determine their stability for on-the-fly variations in output voltage and load. The analysis finds that the three-level converter is more efficient across the full output range, with lower component loss variability compared to the one-phase and two-phase buck converters. However, it suffers from poor dynamic performance with high output deviations and slow response times. The analysis was verified using three prototype converters designed for 200 W, 15 V to 28 V output.**

***Index Terms*—buck, dc-dc, multi level, wide output voltage, medical, modular, isolated, statistical analysis**

I. Introduction

Advances in medical and industrial technologies have driven the demand for power supplies with high standards of safety, reliability, and flexibility [1], [2]. Many industrial and medical products require flexible power sources, but cannot justify the time and capital investment required for a custom power solution due to low production volumes. A commercial off-the-shelf power supply alleviates a lot of these problems, and a design that can be used for a variety of applications increases the potential market while simplifying supply chain requirements [2]–[4]. This can be achieved using an ac-dc isolated modular power supply which can be configured with multiple floating output modules to provide various voltages that can be changed on-the-fly, or connected in series or parallel to provide higher voltages and currents.

Increasing the output voltage range of the modules significantly enhances the flexibility of these power supplies; instead of multiple modules designed to output a relatively small range of voltages, a single module that can provide a wide range of voltage allows for more complex use-cases. Wide output voltage operation is critical for certain applications like capacitor/battery charging, dc motor control and power amplification [5]–[7], where on-the-fly adjustment of the output is critical. In contrast to fixed output power supplies, the difficulty that comes with designing for wide output ranges is providing the rated power efficiently at all voltages and load levels, and ensuring the output remains stable under a variety of output conditions. This makes it impracticable to implement voltage or load specific optimisations that are generally considered in literature [8]–[14].

In the modular power supply considered, there are three main power conversion stages: a central ac-dc rectification and PFC boost stage, a high efficiency isolated resonant dc-dc converter that provides an intermediate bus voltage, and a final regulated dc-dc converter module that may act in parallel or series with other modules. Varying the output voltage could be achieved by modifying the first two stages of power conversion [5], [15]–[20]. However this is not suitable for this particular application since the modules should be able to operate completely independently of each other. Any changes made in the first two power conversion stages would also propagate to the other modules as they all use the same intermediate bus. To maintain independent operation between the modules, this leaves varying the output voltage range of the final dc-dc converter.

This paper evaluates three dc-dc converter topologies as the final conversion stage in a modular ac-dc power supply. The losses generated by the converter and its components, and the dynamic performance are modelled over a wide range of operating conditions to assess their performance. The single-phase (1P, Fig. 1a) buck, two-phase interleaved (2P, Fig. 1b) buck and the three-level (TL, Fig. 1c) buck are assessed in this paper. These and other topologies have not been fully evaluated for wide output voltage applications as most previous research has only looked at a single operating point, at significantly different power range or with a narrow range of outputs [11], [21]–[25]. The 1P buck was selected as a benchmark due to its ubiquity, the TL for its reduced FET voltage stresses and improved switching losses, and the 2P buck for its good high current capabilities and as an intermediary topology. The TL and 2P converters have a similar component count, both have four MOSFETs with one additional passive component compared to the 1P; and inductor for the 2P and a flying capacitor for the TL. The components were selected for a 36 V input, 15 V to 28 V output which corresponds to a wide duty-cycle range of 41.7 % to 77.8 %. The maximum output current is 8.33 A with a peak power of 200 W under normal operation, which follows the specifications of a module from the modular

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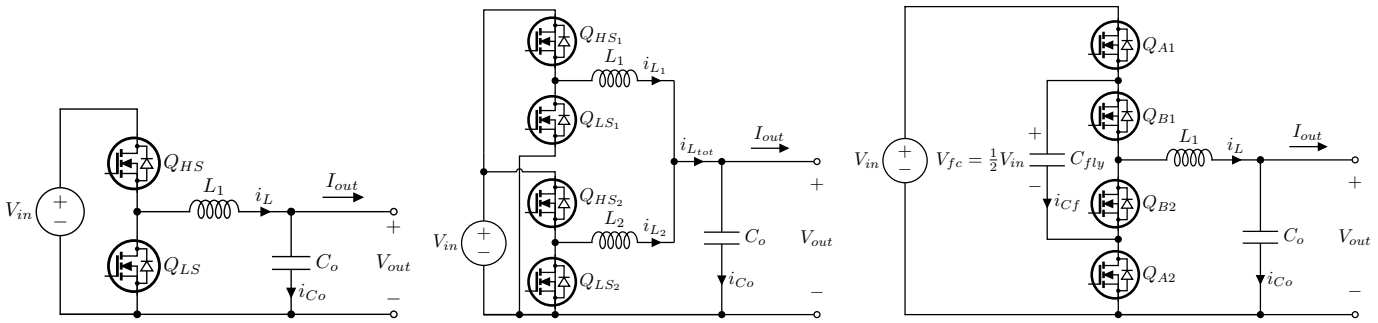


(a) 1P Buck Converter (b) 2P Buck Converter (c) TL Buck Converter

Figure 1: The One Phase (a), Two Phase (b) and Three Level (c) buck converters

power supply considered.

II. Converter & Controller Design

A. Converter Design

Traditionally when comparing topologies, the fundamental switching frequency of the converters is maintained while the area/volume is minimised. For this comparison, a different approach is used where each topology was designed to have the same maximum output voltage ripple in a similar form-factor to enable a like-for-like comparison if the converters were designed to be a drop-in replacement for currently on-the-market technologies.

To maintain the same maximum output voltage ripple while using the same output inductance and capacitance values, the switching frequencies of the converters was modified to exploit the advantages of the topologies; i.e., current ripple cancellation for the 2P, and doubling of frequency and splitting the input voltage for the TL. The 1P operates at 240 kHz, while the 2P and TL operate at 120 kHz and 60 kHz respectively. The switching frequency of the TL was reduced significantly because the switching cycle of the TL effectively doubles the inductor current frequency while also halving the voltage across the inductor. The same inductor is used in the 1P and TL; while the 2P inductors are smaller since the two phases share current, but have the same inductance as the 1P and TL. The flying capacitor in the TL converter must be charged to half the input voltage of the converter before switching begins, and this is achieved by pre-charging the capacitor similar to the implementation by Reusch et al. [26]. The selection of components is detailed in Table I, with some key parameters specified. The MOSFETs in the 1P and 2P converters are the 60 V V_{DS} rated ISC0702NLS, while the TL buck uses the 25 V rated BSC009NE2LS to take advantage of the lower V_{DS} blocking voltage required, allowing the use of MOSFETs with better characteristics compared to their 60 V counterpart; which is one of the main advantages of the TL converter. The MOFETs are driven by the ADuM4121 with a high-side boostrap circuit for the 1P and 2P converters, while the TL converter uses a cascaded bootstrap setup. In order to allow the TL buck to be a drop-in replacement of the 1P, it is imperative that the overall size of the converter be similar to the 1P. Hence the more efficient the TL buck is, the smaller it can be made, increasing power density. Comparing the overall circuit sizes, the 2P and TL have similar footprint areas, while the 1P is 20 % smaller due to fewer components.

B. Converter Controller Design

Stable control of the converters over a wide output voltage range with a variety of load types necessitates a very robust control scheme. Peak current mode control (PCMC) schemes are frequently used [27] as they can limit the inductor current on a cycle-by-cycle basis allowing for a constant-current output, which can be beneficial for handling high capacitance loads or short-circuit conditions compared to voltage mode control (VMC) schemes.

Table I: Converter Component Selection

Component	1P Synchronous Buck	2P Synchronous Buck	TL Synchronous Buck
MOSFETs	$V_{DS} = 60\,\mathrm{V}, \quad R_{DS} = 2.8\,\mathrm{m\Omega}$		$V_{DS} = 25\,\mathrm{V},\ R_{DS} = 0.9\,\mathrm{m\Omega}$
MOSFET Drivers	$V_{GS} = 12\,\mathrm{V}, \quad R_{pu} = 10\,\Omega, \quad R_{pd} = 5\,\Omega$		
Output Capacitor	$1 \times 100\,\mu\mathrm{F}$ (Alu-Elec) $\quad 3 \times 10\,\mu\mathrm{F}$ (MLCC)		
Flying Capacitor	N/A	N/A	$5 \times 10\,\mu\mathrm{F}$ (MLCC)
Inductor	$L = 10.8\,\mu\mathrm{H}, \quad N_{turn} = 5$ $d_w = 1.3\,\mathrm{mm}, \quad$ EQ25/LP	$L = 10.8\,\mu\mathrm{H}, \quad N_{turn} = 7$ $d_w = 0.9\,\mathrm{mm}, \quad 2 \times$ EQ20	$L = 10.8\,\mu\mathrm{H}, \quad N_{turn} = 5$ $d_w = 1.3\,\mathrm{mm}, \quad$ EQ25/LP
Area Estimate	$8.06\,\mathrm{cm}^2$	$11.03\,\mathrm{cm}^2$	$10.65\,\mathrm{cm}^2$
Switching Frequency	240 kHz	120 kHz	60 kHz (120 kHz effective)

Table II: Converter Controller Characteristics

Controller	Gain Margin	Phase Margin	Bandwidth
1P PCMC	10.0 dB	66.4°	22.6 kHz
1P VMC	9.95 dB	43.8°	15.2 kHz
2P PCMC	9.97 dB	65.8°	11.7 kHz
2P VMC	9.96 dB	45.8°	10.7 kHz
TL VMC	9.93 dB	41.4°	6.1 kHz

For the TL converter though, the literature shows there is great difficulty in designing a current mode control scheme for multi-level converters that can operate at certain duty-cycles, or transitioning above/below these duty-cycles [28]–[30]. This is primarily due to the inductor current ripple amplitude approaching zero at certain duty-cycles depending on the number of levels in use. For the TL converter, this occurs at 50 % duty-cycle. Due to this operational limitation and the wide output voltage range requirement of this analysis, only the VMC scheme is implemented in the TL converter, while both PCMC and VMC schemes were implemented for the 1P and 2P converters.

For the TL buck, the modulation scheme described by Da et al. [31] was used for the PWM generation and flying capacitor balancing. The flying capacitor balancing was achieved using an independent low bandwidth PI controller that monitors the flying capacitor voltage V_{fc} and modifies the switching cycle of the converter to charge or discharge the flying capacitor as needed. The converter controllers were designed for the highest bandwidth (to a maximum of 10 % of the fundamental switching frequency) with a phase margin between 40° to 65° and maintaining a minimum gain margin of approximately 10 dB to ensure stability over the full range of outputs. The controllers were implemented digitally with a sampling frequency matching the fundamental switching frequency of the converters. The characteristics of the controllers can be seen in Table II. Since the sampling speed of the controllers is tied to the switching frequency of the converters, for the 2P and TL the bandwidth drops significantly due to the digital transformation causing the phase to drop quickly when approaching half the sampling frequency, which can be seen in Fig. 2. This can significantly limit the maximum gain margin the controller can attain when pushing the bandwidth near the sampling frequency of the controller. Due to these limitations, the VMC schemes have lower phase margin and bandwidth compared to their PCMC counterparts.

III. Analysis

A. Power Losses & Efficiency

To analyse the converters in detail over a wide output range, analytical models and prototype circuits of each of the converters were built using the components specified in Table I, and an example of the prototype converter daughtercard can be seen in Fig. 3. The analytical models calculated the MOSFET losses using [32], and the core and winding losses using [33]. The losses generated by the current shunts, MOSFET

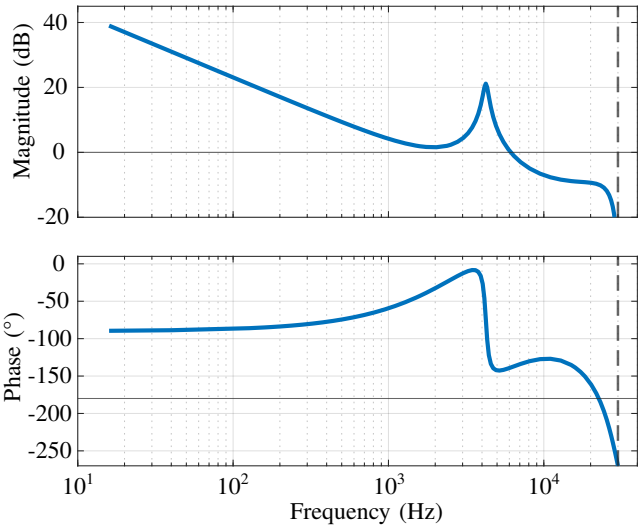


Figure 2: Bode plot of the compensated TL VMC open loop system response

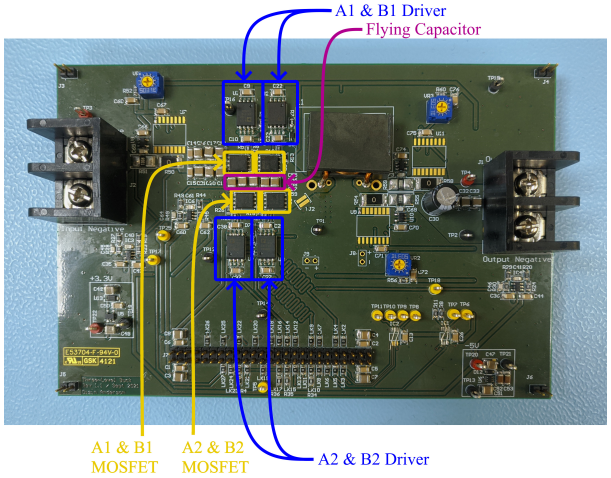


Figure 3: Prototype three-level converter daughtercard

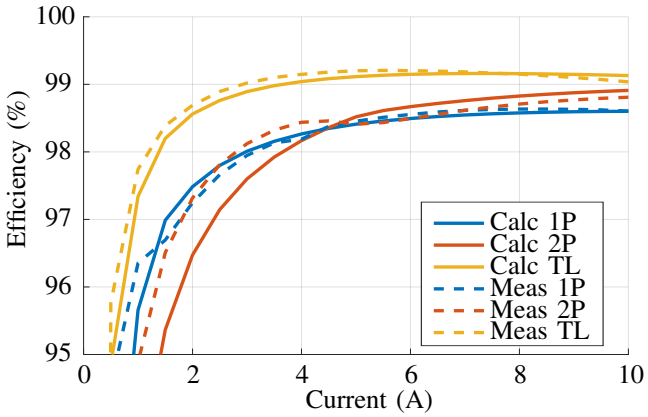
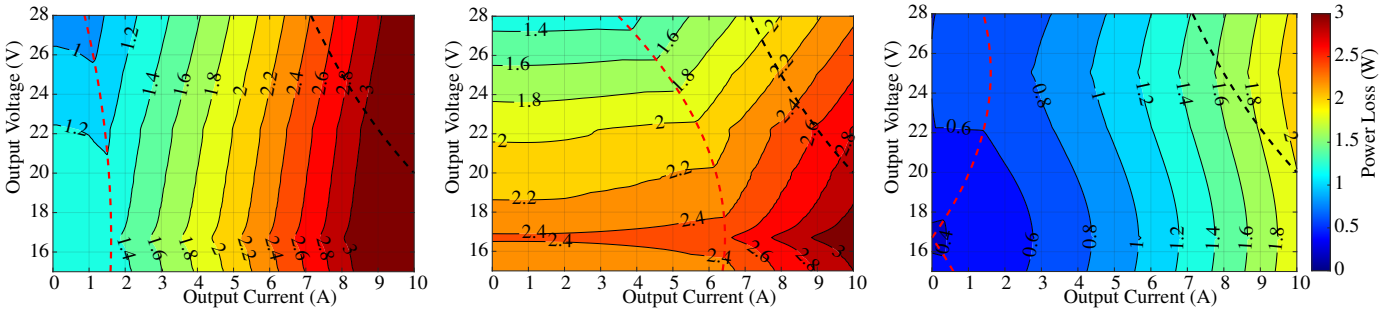
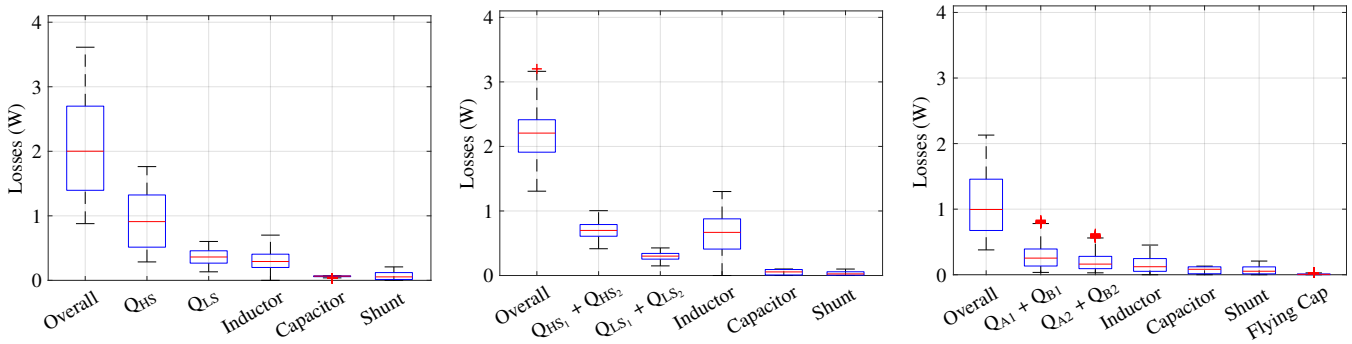


Figure 4: Calculated & measured converter efficiency at 28 V



(a) 1P Converter Heatmap (b) 2P Converter Heatmap (c) TL Converter Heatmap

Figure 5: Heatmap of converter losses. Black line marks 200 W. Red line marks CCM boundary



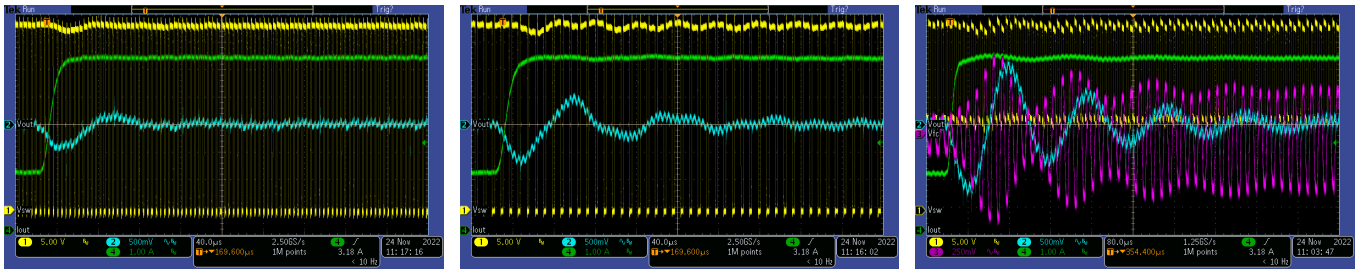
(a) 1P Converter Loss Distribution (b) 2P Converter Loss Distribution (c) TL Converter Loss Distribution

Figure 6: Boxplot of converter losses over all operating points

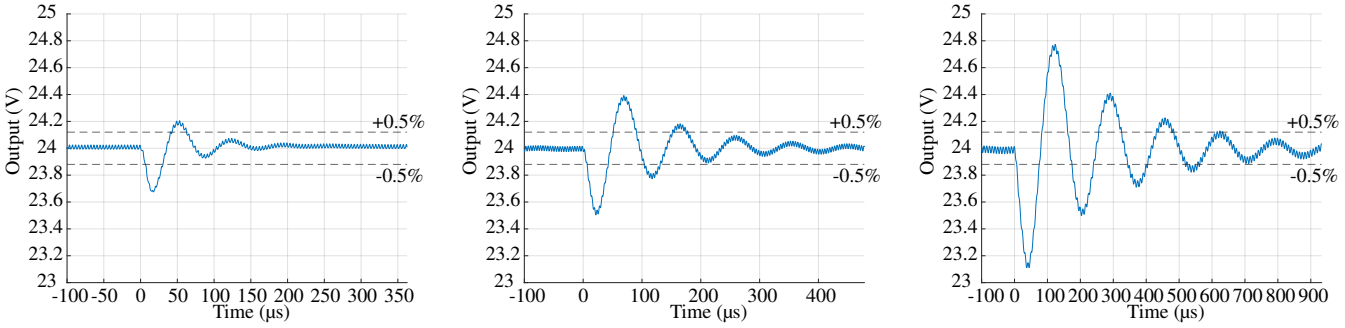
drivers and capacitances are also included. These models assume Forced PWM operation, where the inductor current is allowed to go negative, as the prototypes do not have diode emulation implemented. The design of these models allows the converters to be analysed over a wide range of operating conditions compared to simulating individual operation points in simulation software like LTSpice or PSpice. The measured and calculated efficiency of the converters at 28 V are compared in Fig. 4, and shows good agreement between the calculated and measured efficiency. Due to power supply limitations the input voltage is set to 33.3 V, which is accounted for in the calculations and analysis completed. Figure 4 shows that the TL buck is more efficient than the other two converters at every output current level at a 28 V output. This can be mostly credited to the lower switching losses, from the halved MOSFET V_{DS} and lower switching frequency. Figure 4 only compares the efficiency of the converters at one particular output voltage, so multiple graphs would be required for different output voltages. This can quickly become unintelligible, or inadvertently exclude a certain operating point where efficiency significantly changes. Comparing the converters over a wide range of operating points using efficiency can also become problematic, as the output power levels will significantly skew the efficiency even if the power losses remain constant. Considering that the limiting factor of many designs is the maximum power that can be dissipated by the power supply, this can be avoided by analysing the power loss instead of efficiency over a wide range of outputs.

By computing the losses generated at every operating point, this can be represented on a "heatmap" where all the operating points can be evaluated at once, as shown in Fig. 5. This allows quick determination of the worst operating condition of the converter, and directs where optimisations are required. From the heatmaps, it can be seen that the converters produce higher losses at particular output voltages, which correspond to when the inductor current ripple is at its maximum (50 % duty-cycle for the 1P and 2P converters, 25 % & 75 % for the TL converter). The TL buck has its lowest losses at approximately 16.7 V because it is operating at 50 % duty cycle, where the converter acts more like a switched capacitor converter. The worst case power loss for the TL buck is low at 2.13 W, compared to the 3.61 W and 3.20 W for the 1P and 2P respectively. This near doubling in power dissipated would necessitate a significant increase in heatsink size, which diminishes the benefits of the initially smaller 1P converter design.

To more accurately determine where the optimisation effort should go, a statistical analysis on the contribution of losses over all the operating ranges was completed. Figure 6 shows boxplots detailing the distribution of losses from the converters



(a) 1P VMC Load Step Measured (b) 2P VMC Load Step Measured (c) TL VMC Load Step Measured



(d) 1P VMC Load Step Simulated (e) 2P VMC Load Step Simulated (f) TL VMC Load Step Simulated

Figure 7: Comparison of measured and simulated load step response.

operating at every output voltage and current shown in Fig. 5. These boxplots show the median losses produced by the components, and the variability over the output range of the converter. This makes it clear to identify which components produce the most losses, and also to determine if any components are approaching their operational limits. The median losses of the TL converter are low at 0.98 W compared to 2.0 W and 2.27 W for the 1P and 2P converters respectively. The distribution of losses is significantly different across the topologies. The variability of the losses is also significantly lower in the TL converter, where the difference between the highest and lowest losses are only 1.69 ΔW compared to 2.72 ΔW and 1.91 ΔW for the 1P and 2P converters respectively. The high side MOSFET is the dominating loss in the 1P, while in the 2P converter the inductor losses are the largest contributor with high variability as well. The TL converter on the other hand has a very even distribution of losses across the components, with very little variability.

From these box plots, it is evident that the inductor losses for the TL converter are much lower allowing for a reduction in inductor size, potentially reducing the overall footprint. Combined with the even distribution and smaller deviation of losses also means the TL converter is much easier to manage thermally compared to the worst case high side MOSFET loss with the 1P, which would require significant effort to cool due to the high concentration of heat.

B. Output Regulation

While the efficiency of a converter usually determines the maximum output power, the output regulation influences what kind of loads can be connected to the output. If the output regulation is unreliable, it cannot be used to power sensitive loads or used in high reliability applications. To determine which converter provides the most robust output regulation, the converters were simulated in Simulink using the controllers specified in Table II. To establish which converter topology and control scheme provides the best dynamic performance over a wide range of outputs, the converters were evaluated by measuring the load transient and voltage step characteristics.

To verify the performance of the controllers, the load step response of the VMC converters were measured and compared against the simulated response. A comparison of measured and simulated responses can be seen in Fig. 7. The voltage at the connection between the MOSFETs and the inductor is shown in yellow (Ch.1, 5.0 V/div), the ac component of the output voltage is shown in blue (Ch.2, 500 mV/div), the output current in green (Ch.4, 1.0 A/div), and the ac component of the flying capacitor voltage is shown in purple (Ch.3, 250 mV/div) for the TL converter. The oscilloscope time base is 40 µs/div

Table III: Converter load transient performance, I_{out} 25 % to 75 % at 24 V V_{out}

Controller	Overshoot	Undershoot	T_s ±0.5 %
1P PCMC	0.10 %	−1.29 %	106 µs
1P VMC	0.85 %	−1.35 %	62.5 µs
2P PCMC	0.07 %	−2.41 %	167 µs
2P VMC	1.63 %	−2.07 %	178 µs
TL VMC	3.22 %	−3.70 %	633 µs

Table IV: Converter voltage step performance, V_{out} 15 V to 28 V at 7.14 A I_{out}

Controller	Overshoot	T_r 10 %→90 %	T_s 90 %→±0.5 %
1P PCMC	0.14 %	356 µs	421 µs
1P VMC	27.17 %	31.4 µs	510 µs
2P PCMC	0.10 %	194 µs	274 µs
2P VMC	17.0 %	23.4 µs	645 µs
TL VMC	1.0 %	227 µs	828 µs

for the 1P and 2P, but 80 µs/div for the TL converter. The measured results show similar performance to the simulated response, although the overshoot and undershoot amplitudes are typically 20 % to 45 % higher than the simulated response. This can be attributed to unaccounted delays in the converter microcontrollers, and other mismatches between the physical components and the idealised simulated components.

For the load transient analysis, the converters were stepped from 25 % to 75 % of their maximum designed output current (8.33 A). The voltage deviation from nominal (24 V) and time to settle (±0.5 % of nominal) was measured when the output load was stepped. From Table III it can be seen that while PCMC usually has a longer settling time compared to an equivalent VMC scheme, it has practically no overshoot and a smaller peak to peak deviation. This is often more desirable than a fast response in high reliability applications where consistency and predictability is critical. In this particular comparison, the settling time of the 2P VMC converter is slightly longer than the 2P PCMC because the oscillations are not as well damped, and so slightly goes over the 0.5 % threshold technically extending the settling time.

Of the three topologies, the 1P buck converters have the best transient performance followed by the 2P converters with roughly double the voltage deviation. The TL converter increases the voltage deviation again to 6.92 %, with a long settling time of 633 µs due to large oscillations from the lower phase margin. The slow dynamic performance of the TL can be attributed to the low bandwidth of the controller, as well as the output filter resonance occurring near the desired bandwidth which was not ideal for converter compensation. If the output filter was modified and the switching frequency increased for similar output voltage ripple, the dynamic performance could be improved.

For the voltage step analysis, the converters were commanded to step from their minimum to maximum output voltage. The V_{out} 10 % to 90 % rise time was measured, as well as the overshoot and settling time from V_{out} 90 % to ±0.5 % of the final voltage. Table IV shows similar results to the load transient testing, where the 1P converter has the fastest settling time with no overshoot when using the PCMC scheme. The VMC converters have an undershoot of −31.0 %, −48.0 % and −9.24 % for the 1P, 2P and TL converters respectively, while the other PCMC schemes have an undershoot of approximately −2.1 %. The rise time of the PCMC converters is slower than theoretically possible (particularly the 1P converter) due to the anti-windup implementation, which limits the maximum current through the inductors. Since the current was shared across two inductors for the 2P converter, the anti-windup measures didn't affect the rise time as significantly as the 1P converter. Generally, the VMC schemes have very fast rise times at the cost of overshoot and high peak currents, while the PCMC is slower but has a monotonic rise to the final voltage. The TL converter has the worst performance again, with a very slow rise time and long settling time. While the TL converter has relatively low overshoot, its rise was not monotonic with some oscillations while rising due to the controller operating near the resonance of the output filter. The slow performance of the TL converter could be improved with a peak/valley current mode control scheme, but currently many of these implementations only allow operation within narrow duty-cycle ranges.

IV. Conclusion

This paper presents an evaluation of three dc-dc converter topologies for wide output voltage applications.

Analysis of the losses shows that over a wide range of conditions in a like-for-like configuration, with similar peak efficiency of the converters at 99 %, 98.5 % and 98.9 % for the TL, 1P and 2P converters respectively. From the statistical analysis of the losses at every operating point, the median losses produced were significantly lower in the TL converter at 0.98 W compared to 2 W and 2.27 W for the 1P and 2P converters respectively. The variability of the losses is also significantly lower in the TL converter, where the difference between the highest and lowest losses were only 1.69 ΔW compared to 2.72 ΔW and 1.91 ΔW for the 1P and 2P converters respectively.

When comparing the dynamic performance of the converters, the opposite trend appears where the 1P converter and 2P converters outperform the TL converter. The 2P converter has faster rise times compared to the 1P converter when changing output voltage. The TL converter suffers from much worse dynamic performance due to the difficulty in implementing current mode control over the full duty-cycle range, limiting it to only voltage mode control with additional circuitry to monitor the flying capacitor voltage. Overall, if efficiency is critical the three-level converter is the best option thanks to its lower switching frequency while still maintaining similar output voltage ripple. If dynamic performance is more important, it would be worthwhile decreasing the system efficiency by using the 1P or 2P for a much higher bandwidth system. Increasing the switching frequency of the TL converter could improve the dynamic performance, but might eliminate the efficiency benefits of the topology. A similar comparison of the converters with the same fundamental switching frequency but with optimised components will be investigated in the future.

References

[1] D. Howes, "What is Modular Configurable Power? - Technical Articles," 2020. [Online]. Available: https://eepower.com/technical-articles/when-a-modular-power-supply-is-the-best-solution/

[2] B. Schweber, "Off-The-Shelf Medical Power Supplies — DigiKey," 2022. [Online]. Available: https://www.digikey.com/en/articles/select-the-right-ac-dc-power-supply-to-meet-unique-medical-requirements

[3] "Off-the-shelf Power Supplies Simplify System Design — RECOM," 2022. [Online]. Available: https://recom-power.com/en/rec-n-off-the-shelf-power-supplies-simplify-system-design-212.html?0

[4] C. Jones, "Understanding the real benefits of flexibility and configurability in power systems design." [Online]. Available: https://artesyncom-prod.scdn8.secure.raxcdn.com/assets/configurable_white_paper_r3_1_1367959072_WP.pdf

[5] M. I. Shahzad, S. Iqbal, and S. Taib, "A wide output range HB-2LLC resonant converter with hybrid rectifier for PEV battery charging," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 2, pp. 520–531, 2017.

[6] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151–2169, 2013.

[7] P. F. Miaja, M. Rodríguez, A. Rodríguez, and J. Sebastián, "A linear assisted DC/DC converter for envelope tracking and envelope elimination and restoration applications," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3302–3309, 2012.

[8] O. Kirshenboim and M. M. Peretz, "High-Efficiency Nonisolated Converter With Very High Step-Down Conversion Ratio," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3683–3690, may 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7508455/

[9] K. Yao, Y. Qiu, M. Xu, and F. C. Lee, "A novel winding-coupled buck converter for high-frequency, high-step-down dc-dc conversion," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1017–1024, sep 2005.

[10] G. Li and X. Wu, "High power density 48-12 v DCX with 3-D PCB winding transformer," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1189–1193, feb 2020.

[11] J. W. Kwak and D. Brian Ma, "Comparative Topology and Power Loss Analysis on 48V-to-1V Direct Step-Down Non-Isolated DC-DC Switched-Mode Power Converters," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, Oct. 2020, pp. 943–949.

[12] M. Choi and D.-K. Jeong, "18.6A 92.8%-Peak-Efficiency 60A 48V-to-1V 3-Level Half-Bridge DC-DC Converter with Balanced Voltage on a Flying Capacitor," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, vol. 2020-Febru. IEEE, feb 2020, pp. 296–298. [Online]. Available: https://ieeexplore.ieee.org/document/9063061/

[13] R. Das and H.-P. Le, "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2019-March. IEEE, Mar. 2019, pp. 1997–2001.

[14] G. S. Seo, R. Das, and H. P. Le, "A 95%-Efficient 48V-to-1V/10A VRM Hybrid Converter Using Interleaved Dual Inductors," in *2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018*. Institute of Electrical and Electronics Engineers Inc., dec 2018, pp. 3825–3830.

[15] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range; A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," Tech. Rep., 2005.

[16] H. G. Han, Y. J. Choi, S. Y. Choi, and R. Y. Kim, "A High Efficiency LLC Resonant Converter with Wide Ranged Output Voltage Using Adaptive Turn Ratio Scheme for a Li-Ion Battery Charger," in *2016 IEEE Vehicle Power and Propulsion Conference, VPPC 2016 - Proceedings*. Institute of Electrical and Electronics Engineers Inc., dec 2016.

[17] X. Wu, Z. Bai, and H. Ma, "An LLC Converter Operating in Super-Wide Output Voltage Range with Variable-Mode Control Strategy," in *Proceedings - 2018 IEEE International Power Electronics and Application Conference and Exposition, PEAC 2018*. Institute of Electrical and Electronics Engineers Inc., dec 2018.

[18] W. Ye, W. Cui, S. Shao, J. Zhang, and K. Sheng, "A Resonant DC-DC Converter with Modular Rectifier for High Voltage Gain and Wide Output Voltage Range Applications," in *IECON Proceedings (Industrial Electronics Conference)*, vol. 2019-Octob. IEEE Computer Society, oct 2019, pp. 6671–6676.

[19] M. Shang and H. Wang, "A Voltage Quadrupler Rectifier Based Pulsewidth Modulated LLC Converter with Wide Output Range," *IEEE Transactions on Industry Applications*, vol. 54, no. 6, pp. 6159–6168, nov 2018.

[20] F. Musavi, M. Craciun, D. S. Gautam, and W. Eberle, "Control strategies for wide output voltage range LLC resonant DC-DC converters in battery chargers," *IEEE Transactions on Vehicular Technology*, vol. 63, no. 3, pp. 1117–1125, 2014.

[21] M. D. Seeman, V. W. Ng, H.-P. Le, M. John, E. Alon, and S. R. Sanders, "A comparative analysis of Switched-Capacitor and inductor-based DC-DC conversion technologies," in *2010 IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, Jun. 2010, pp. 1–7.

[22] J. P. M. Figueiredo, F. L. Tofoli, and R. L. Alves, "Comparison of nonisolated dc-dc converters from the efficiency point of view," in *XI Brazilian Power Electronics Conference*. IEEE, Sep. 2011, pp. 14–19.

[23] M. Gleisner and M.-M. Bakran, "Comparison of multiphase versus multilevel DC/DC-converters for automotive power," in *2013 15th European Conference on Power Electronics and Applications (EPE)*. IEEE, Sep. 2013, pp. 1–10.

[24] A. Abdulslam, S. H. Amer, A. S. Emara, and Y. Ismail, "Evaluation of multi-level buck converters for low-power applications," in *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2016-July. Institute of Electrical and Electronics Engineers Inc., jul 2016, pp. 794–797.

[25] C. Carstensen and J. Biela, "A Three-Level Buck Converter with a Wide Voltage Operation Range for Hardware-in-the-Loop Test Systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6176–6191, sep 2016.

[26] D. Reusch, F. Lee, and X. Ming, "Three level buck converter with control and soft startup," in *2009 IEEE Energy Conversion Congress and Exposition*. IEEE, Sep. 2009, pp. 31–35.

[27] R. Mammano, "Switching Power Supply Topology Voltage Mode vs. Current Mode by: Robert Mammano," Tech. Rep., 1994.

[28] E. Abdelhamid, G. Bonanno, L. Corradini, P. Mattavelli, and M. Agostinelli, "Stability Properties of the 3-Level Flying Capacitor Buck Converter Under Peak or Valley Current Programmed Control," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8031–8044, 2019.

[29] E. Abdelhamid, L. Corradini, P. Mattavelli, G. Bonanno, and M. Agostinelli, "Sensorless stabilization technique for peak current mode controlled three-level flying-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 35, pp. 3208–3220, 3 2020.

[30] N. Vukadinović, A. Prodić, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Skip-duty control method for minimizing switching stress in low-power multi-level dc-dc converters," *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics, COMPEL 2015*, 9 2015.

[31] S. da Silva Carvalho, M. Halamicek, N. Vukadinovic, and A. Prodic, "Digital PWM for multi-level flying capacitor converters with improved output resolution and flying capacitor voltage controller stability," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, jun 2018.

[32] X. He, D. Li, and V. Zhang, *An Accurate Approach for Calculating the Efficiency of a Synchronous Buck Converter Using the MOSFET Plateau Voltage*, 2020. [Online]. Available: https://www.ti.com/lit/an/slvaeq9/slvaeq9.pdf

[33] W. Hurley and W. Wölfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications*, ser. Ingenieria electrica. John Wiley & Sons, Apr. 2013.