Impact of DC-DC Converter Topologies on Passive Components Miniaturization

by

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Abstract

Power electronic circuits are a key player in many essential electrical systems and applications, e.g., power converters. For computational and battery-powered consumer products, the desire for higher power densities and longer battery life increases the requirement for smaller, more power-efficient devices. Therefore, these requirements drive the research towards exploring different areas to improve the power converters like circuit topologies, integration, and technologies of the semiconductor devices and passive components.

One of the main challenges in the power converter is the significant contribution of the passive components, particularly magnetics, to the overall solution losses and size. Understanding the different topologies requirement of the passive components for a given load requirement can lead to better utilisation of the passive components, hence, to optimise the passive components, particularly inductors from the circuit perspective, which can reduce the manufacturing materials consumption.

This study proposes design procedures to optimise the utilisation of passive components in DC-DC power converters, particularly inductors. It presents a detailed analysis of passive components in the converter topologies of multiphase buck, multiphase 3-level and single-phase buck with 4^{th} order resonance output filter. This study emphasises the passive components' performance in terms of size and efficiency, besides considering the utilisation of coupled inductors in these circuits and the selection of coupling factor. Air-core PCB integrated inductors are considered in this study for fast prototyping and testing. However, this study is also applicable for inductors with the magnetic core.

This study addresses the impact of the number of phases in multiphase interleaved buck and 3-level topologies on the passive components' energies in wide input voltage converters, in addition to the impact of the PCB design rules on the manufactured inductors' performance, which all combines for better utilisation of the passive components. The study also provides a detailed analysis and selection procedure of passive components in a buck converter with 4^{th} order and 4^{th} order resonance (4thRes) filters for a given converter specification. The novel 4thRes analysis presents its potential in reducing the size of the passive components and the converter's full load efficiency. These contributions help improve the passive components, particularly the inductors, in

terms of power density and performance in low power converters with a wide input voltage range.

These contributions help improve the passive components, particularly inductor, power density and performance in low power converters with wide input voltage.

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Declaration of Authorship

I, Youssef Kandeel, declare that this thesis titled, “Impact of DC-DC Converter Topologies on Passive Components Miniaturization” and the work presented in it is my own. I confirm that: This work was done wholly or mainly while in candidature for a research degree at this university.

- Where any part of this thesis has previously been submitted for degree or any other qualification at this university or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all the main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signature: _____

Youssef Kandeel

Date: _____

List of Publications

Journal Publications

- **Y. Kandeel**, S O'Driscoll, C. O'Mathuna, and M. Duffy, "Optimum Phase Count in a 5.4 W Multiphase Buck Converter Based on Output Filter Component Energies," *IEEE Transactions on Power Electronics,* 2022. **(Under review)**
- **Y. Kandeel**, S O'Driscoll, C. O'Mathuna, and M. Duffy, "Design Procedure for Reduced Filter Size in a Buck Converter Using a 4th Order Resonance Filter," *IEEE Transactions on Power Electronics*, 2022. **(Accepted)**
- C. Shetty, **Y. Kandeel**, L. Ye, S O'Driscoll, P. McCloskey, M. Duffy, and C. O'Mathuna, "Analytical Expressions for Inductances of 3D Air Core Inductors for Integrated Power Supply," *Journal of Emerging and Selected Topics in Power Electronics*, 2021.

Conference Publications

- **Y. Kandeel** S O'Driscoll, C. O'Mathuna, and M. Duffy, "Multiphase 3-Level Buck Passives Analysis Including 2-Phase Coupled Inductors," *2022 IEEE Applied Power Electronics Conference and Exposition (APEC),* Houston, TX, USA, 2022. **(Accepted)**
- **Y. Kandeel** and M. Duffy, "Design of 4th Order Resonance Filter for 5.4 W 20 MHz Buck Converter with PCB Integrated Inductor," *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL),* Aalborg, Denmark, 2020, pp. 1-7.
- **Y. Kandeel** and M. Duffy, "Comparison of Coupled vs. Non-Coupled Microfabricated Inductors in 2W 20MHz Interleaved Buck Converter," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC),* Anaheim, CA, USA, 2019, pp. 2638-2645.

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List of Abbreviations

CMOS	Complementary Metal-Oxide Semiconductor
DAB	Dual Active Bridge
DIMO	Dual Inductor Multiple Output
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FCML	Flying Capacitor Multilevel
FEA	Finite Element Analysis
FET	Field Effect Transistor
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
IC	Integrated Circuit
IVR	Integrated Voltage Regulator
MIM	Metal-Interposer-Metal
MISO	Multiple Input Single Output
MOM	Metal-Oxide-Metal
PCB	Printed Circuit Board
PTH	Plated Through Hole
PwrSiP	Power Supply in Package
PwrSoC	Power Supply on Chip
PWM	Pulse Width Modulation
SC	Switched Capacitor
SIMO	Single Inductor Multiple Output
SMPS	Switch Mode Power Supply
THV	Through-Hole Via
VRM	Voltage Regulator Module
ZVS	Zero Voltage Switching

Chapter 1 – Introduction

1.1 *Overview*

Power electronic circuits and components are significant performers in many fundamental electrical systems, like power converters and motor drives. The power converter is an essential element in many applications, e.g. converting a battery voltage to a suitable level for powering sensors, microprocessors, FPGAs, displays, communication modules, and memory in mobile phones and computers. It is also essential for the multistage conversion of the mains voltage to power Graphical Processing Units (GPU), which are widely used in heavy load workstation computers and cryptocurrency mining computers, among many other applications. The market demands for higher performance or more energy savings in many power electronics applications drives researchers and manufacturers to find solutions for shrinking the volume or improving the efficiency and energy saving of the power converter. Developing a more compact and miniaturised power converter is an endless challenge, considering the manufacturing capabilities and material characteristics. Therefore, research on optimising the size and performance of the power converter and its components is a competitive requirement in the industry. Hence, the size reduction of passive components in the power converters - especially magnetic components - is essential to reduce the overall size of the converter and achieve higher power densities.

1.2 *Background*

Typical power converters are of the Switched Mode Power Supply (SMPS) type, which relies on power semiconductor elements for switching and passive elements, e.g. inductors, transformers, coupled inductors and capacitors [1]. SMPS are found with different scales of integration, e.g.:

- All components are discrete onboard, e.g. as in [2] and shown in Fig. 1.1. This is commonly found in power converters switching in the kHz range. However, it can be used for prototype research converters switching up to 20 MHz with some challenges relating to layout optimisation and inductor current sensing accuracy. More generally, it may be unsuitable for multi MHz frequencies as the impedance of the interconnections becomes more significant. Besides, electromagnetic field radiations and induced currents between system elements will become more

influential, i.e. Electromagnetic Interference (EMI), which can impact the converter performance.

- Power Supply in Package (PwrSiP) where switches and gate drivers are integrated on a silicon chip with some passive components co-packaged on the copper lead frame or interposer, e.g. as in [3], [4] and shown in Fig. 1.2.
- Power Supply on Chip (PwrSoC) where switches, gate drivers and passive components are all integrated on the silicon chip, e.g. as in [5]–[9] and shown in Fig. 1.3.

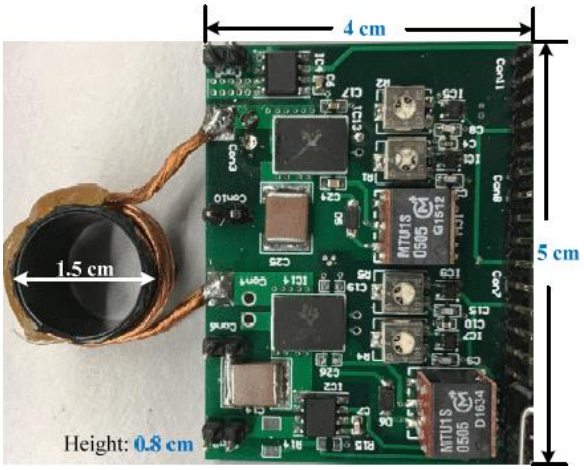


Fig. 1.1 Discrete bidirectional 10 MHz DC-DC converter [2].

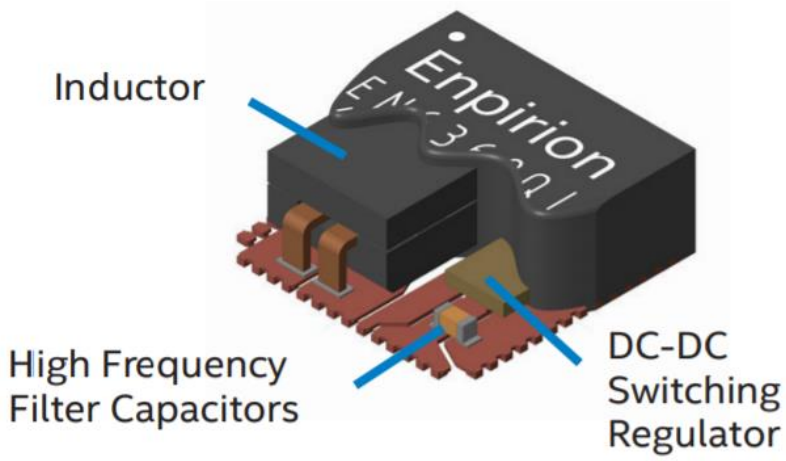


Fig. 1.2 PwrSiP buck converter structure example [3].

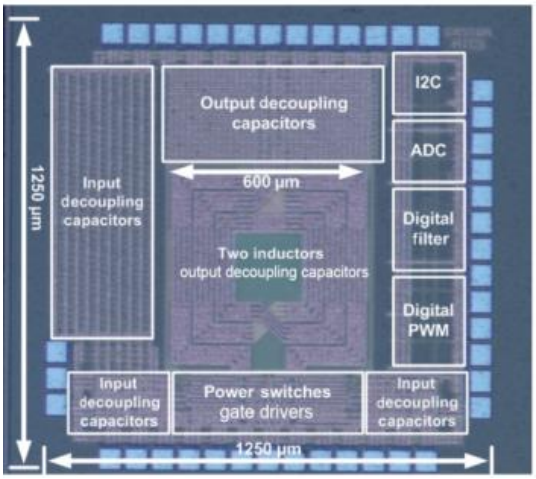


Fig. 1.3 2-Phase 500 MHz PwrSoC buck converter [5].

PwrSiP and PwrSoC are commonly targeted in low power applications where high power density is a competitive requirement, especially in portable devices. However, there are various challenges to achieving high power density, which are:

- Semiconductor technology:
    - Silicon on CMOS is the most common technology process for high-frequency switching devices. Limitations to improving the devices' performance include conduction and switching losses, and the body diode charge recovery, which are limited by fundamental silicon material properties and the MOSFET structure. However, GaN technology has shown promising performance due to its better electron mobility; although, power converters based on the present commercial GaN transistors are limited in frequency < 20MHz.
- Size of the passive components:
    - Usually, inductors carry larger currents than capacitors in the power converter; therefore, size reduction of inductors (and transformers) is more challenging. Inductor size reduction could be achieved by reducing the peak energy required by the inductor by choosing a suitable circuit topology, or by having a higher inductor density. Inductors consist of two main components, the winding and the magnetic core. So, improving the inductor density can be achieved by optimising the winding structure and improving the magnetic core material properties considering the manufacturing technology limitations.

- Capacitors in general have higher energy density than inductors, especially silicon-integrated capacitors such as deep trench capacitors [10], metal-oxide-semiconductor (MOS) capacitors [8], metal-oxide-metal (MOM) capacitors [11], metal-interposer-metal (MIM) capacitors [6][12][13][14]. This encourages researchers to investigate inductorless converter topologies like Switched Capacitors (SC) (in some contexts called "charge pump"); however, they may have challenges relating to output voltage regulation.

- Component interconnections:
  - Improving the PwrSiP and PwrSoC performance and density requires shrinking the length of component interconnections as their impedance becomes more significant as frequency increases. This can be improved through vertical stacking of the converter components as in [15] shown in Fig. 1.4.
- PCB / package / chip manufacturing process capabilities:
  - The manufacturing process imposes limitations on the design of the components and the power converter layout, such as minimum copper width/spacing, minimum drill hole, available copper/PCB thickness, the minimum distance between components/vias/copper tracks, etc. These process limitations restrict shrinking the size of the components.
- Cooling of the components:
  - High-density devices may suffer from 'hot spots' caused by thermally trapped/accumulated power losses within the components, which can affect the converter performance. However, this is not within the scope of this research.

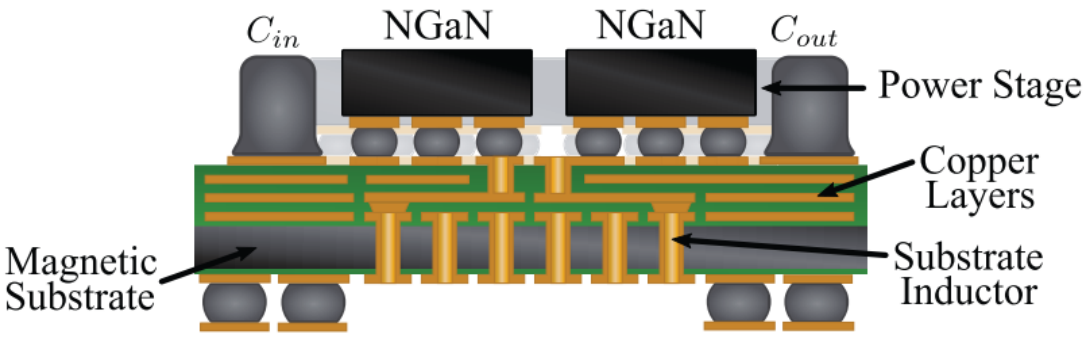


Fig. 1.4 Integrated Voltage Regulator (IVR) stack-up [15].

1.3 *Research problem*

It is widely agreed in the power converter industry that the reduction of the magnetic components is essential towards fulfilling the market requirement of improving the converter power density. However, various application requirements, circuit topologies, and component technologies make it complicated to answer the question, "which DC-DC converter topology utilises the magnetic components the best for given converter specifications?" as there are countless possibilities of outcomes as illustrated in Fig. 1.5.

Taking a voltage regulator for a microprocessor as an example. First, there are multiple power converter topology options, each of which has several design variations, like the number of phases in multiphase topologies, which is commonly investigated for microprocessors. Then, there are multiple inductor structure options; each one has different characteristics, e.g. the toroid structure can achieve higher inductance than the solenoid structure because it encapsulates the magnetic fields better; however, it may be limited more by magnetic core saturation. The choice of magnetic core material based on available characteristics and geometries adds to the complexity of the design selection, especially for custom designed inductors. Finally, the inductor manufacturing technology capabilities can affect the inductor design and the magnetic material handling, which requires a comprehensive design procedure to optimise the inductor performance.

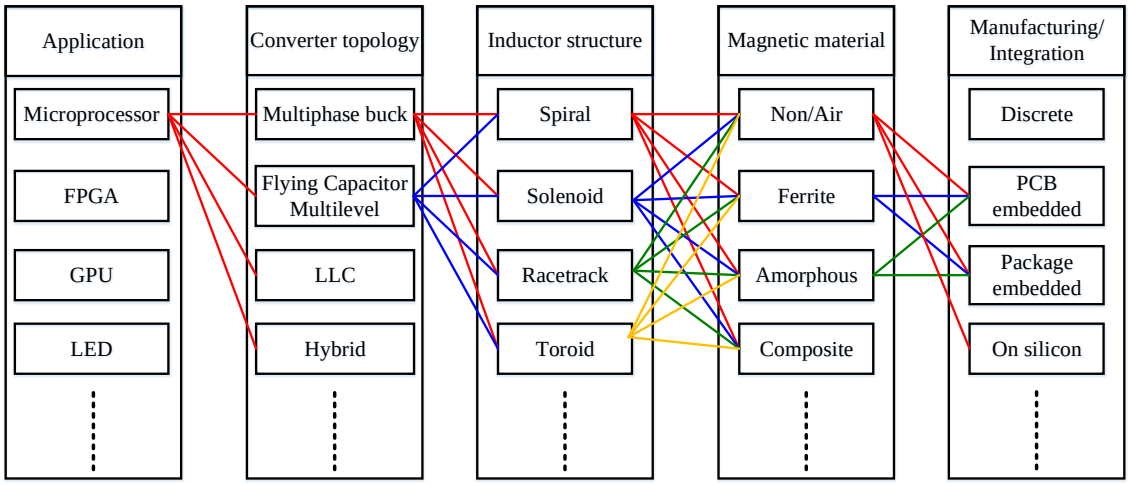


Fig. 1.5 Illustrative example of the countless combinations of the power converter ingredients from magnetic component perspective.

To improve the performance of the passive components in the power converter, some researchers use numerical optimisation techniques, e.g. as in [16]. However, this procedure may not offer comprehensive insight into the converter topology architecture's impact on the performance of the passive components. Besides, it adds the requirement

of a software tool and optimisation script, which may increase the complexity of designing a power converter.

This highlights the necessity for a design procedure/philosophy for DC-DC converter topology selection to optimise the utilisation of the magnetic components while being flexible to accommodate different component technologies.

1.4 *Research Objectives*

This research aims to assess the impact of DC-DC converter topology architectures on the size and performance of the passive components, particularly inductors, for more optimum utilisation of these components. The focus is on low power converters switching at multi mega Hz frequencies. This leads to better understanding of the converter topology selection in terms of its potential for converter size reduction and/or increased energy saving. Reduced size may result in reduced consumption of manufacturing materials, potentially reducing the cost of mass production and its associated environmental impact.

The proposed procedure investigates the passive components in various circuit topologies for given converter specifications, referring to a baseline topology (e.g. the single-phase buck), and verifying the level of improvement in converter performance with the selected passive components. There are many circuit topologies for DC-DC converters (including their derivatives); therefore, the most commonly used topologies for low power applications are selected to address the research objective challenges. Converters employing coupled inductors have other challenges, especially with a wide input voltage range, which adds to the complexity of the inductor selection. The passive components' peak energy is the initial theoretical parameter to evaluate the relative size of the components for each topology. Then, the limitations of inductor and capacitor manufacturing technologies and materials that can significantly impact initial predictions are considered.

This study focus on the converter topologies of the multiphase interleaved buck, the multiphase interleaved 3-Level, and a buck converter with a 4^{th} order resonance low pass output filter. The application of coupled inductors in these topologies is also considered. The analysis throughout the thesis is applied mainly to a typical step-down Point-of-Load (POL) DC-DC converter specification; i.e. output power of 5.4 W, switching frequency

of 20 MHz with a wide input voltage range and practical limitations on converter operation, e.g. current ripple per phase.

To investigate the influence of the converter topologies on the inductor size and losses, air-core PCB integrated inductors are considered for manufacturing and testing with the prototype converter; this avoids the complexities related to the magnetic core material characteristics and core loss nonlinearities. The prototype converter is implemented with Gallium Nitride (GaN) FET transistors for its capability for fast switching.

Research objectives are summarised as follows:

- Identify the impact of the number of phases in multiphase interleaved buck and 3-level buck topologies on the passive component values, peak energy and size.
- Identify the effect of restricting the inductor current ripple in each phase of a multi-phase interleaved topology on the passive components size and performance.
- Provide a procedure for selecting a suitable coupling factor for a two-phase coupled inductor for wide input voltage specifications in multiphase buck and 3-level topologies.
- Provide a passive components selection procedure for 4^{th} order and 4^{th} order resonance output filters for a given buck converter specification.
- Identify the impact of the 4^{th} order and 4^{th} order resonance output filters on passive components in a buck converter compared to the standard 2^{nd} order filter.
- Identify the effect of the PCB manufacturing process limitations on the inductor size hence on the topology selection.
- Compare the passive components required by the studied topologies for different converter specifications.

This study will contribute to optimising the DC-DC converter topology selection by evaluating the utilisation of the passive components and considering their manufacturing process capabilities. This will help improve the converters' power density and optimise the required amount of materials for the passive components. That concept of topology selection can be beneficial to cost reduction and the environment. It also opens the door to more research in the power converter topology selection to reduce material consumption.

More significantly, there is a potential for improved efficiency, especially in low-power applications, which are integrated into various portable electronic products. These products are in widespread and growing use throughout the world, and therefore the accumulated energy savings can be significant.

This research has some limitations, such as considering the semiconductors' scaling in the presented topology selection procedure. Another key limitation is the fact that there are numerous combinations of applications, converter topologies, inductor types and magnetic core materials, which requires research effort and time beyond this study. Therefore, findings are specific to certain topologies and particular inductor technologies.

1.5 *Thesis Structure*

This thesis is structured as follows:

Chapter 1: Introduction

This chapter presents the study context, overview and challenges. The research objectives are identified, and the significance of this research is highlighted. The study limitations have been discussed as well.

Chapter 2: Literature Review

This chapter presents a review of the state of the art of power converters operating at relatively high switching frequencies and low output power, which are suitable for integration within a package or on silicon, i.e., PwrSiP or PwrSoC. It compares different aspects of the power converters' topologies, electrical specifications, integration technology, magnetic component types and integration, and semiconductor technology. The review highlights the most interesting converters in terms of these aspects. The challenging power converter metrics are concluded at the end of this chapter.

Chapter 3: Multiphase Buck Topology

This chapter provides a normalised analysis of passive components in a multiphase interleaved buck converter for given specifications and considers assumptions of practical converter limitations. It also presents a 20 MHz converter implementation with GaN FET switches and air-core PCB integrated solenoid and spiral inductors. Moreover, it provides a guideline for coupling factor selection of a 2-phase coupled inductor in a multiphase buck converter.

Chapter 4: Multiphase 3-Level Topology

Similar to chapter 3, this chapter provides an analysis of passive components in a multiphase interleaved 3-Level converter. It also presents the scaling of the 2-phase coupled inductor analysis for the multiphase 3-Level topology. In this chapter, five converter designs are selected for performance investigation and comparison in terms of passive components' size, steady-state efficiency performance, and load transient performance.

Chapter 5: 4th Order Resonance Output Filter Topology

This chapter presents an in-depth analysis and novel design procedure of a buck converter with 4th order and 4th order resonance output filters based on Butterworth normalised filters, and shows a comparison against the standard 2nd order LC filter in terms of the overall passive component requirements. Air-core PCB integrated solenoid inductors are considered for implementation and testing for these filters. Moreover, employing coupled inductors in a 4th order resonance filter is also discussed.

Chapter 6: Discussion and Topologies Comparison

This chapter discusses the general findings and trade-offs of the converter topologies investigated in the previous chapters. To illustrate the scope of the findings, the same analysis is applied to three other converter specifications.

Chapter 7: Conclusions

This chapter summarises the main findings and the proposed research areas for future work.

1.6 *Thesis Contributions*

The thesis's main contributions are as follows:

- Presenting a literature review focused on recent low-power high-frequency DC-DC converters. Converters are compared based on various topology and inductors metrics, and the highest performing converters are identified and highlighted.
- Explaining the impact of the multiphase buck topology in terms of increasing the number of phases on the passive components' performance, while accounting for practical input voltage ranges and limited inductor currents within each phase.

- Extending the analysis to identify the multiphase 3-level topology impact of the passive components compared to the multiphase buck topology.
- Presenting coupling factor selection guidelines for a two-phase coupled inductor in the multiphase buck and 3-level topologies.
- Detailed analysis and design procedure of the 4^{th} order and 4^{th} order resonance low pass output filters for a given buck converter specifications, showing this filter's potential to reduce the size and full load loss.
- Comparing the investigated topologies designing according to the proposed procedure against the existing literature for different applications.

Chapter 2 – Literature Review

2.1 *Introduction*

This review aims to identify developments in DC-DC power converters operating at very high frequency and employing miniaturized inductors, as part of the path towards more efficient integration of power converter components and circuitry with reduced size, power loss and heat dissipation. This review focuses mainly on the converters' performance parameters; however, inductor data is also included in the scope. It identifies challenges and opportunities for DC-DC power converter development and outlines suitable circuit topologies and targeted converter specifications.

Publications reviewed range from years 2010 to 2021. Converter data of interest include circuit topology, fabrication technology, switching frequency, input/output voltage, output current, output power, peak efficiency, size/footprint area, and power density. Circuit control parameters, transient response, and thermal characteristics are not within the scope of this review. Upcoming sections presents discussions and comparisons of the collected data.

2.2 *Circuit topology*

DC-DC power conversion can be achieved using various circuit topologies. Voltage step-down is the common operation required in high-frequency power-supply-on-chip (PwrSoC) applications, so most research is focused on circuitry based on the buck topology, including multiphase, cascode, coupled inductors, Single Input Multiple Output (SIMO) and Switched Capacitor (SC) topologies; in addition to combinations of different topologies (e.g. SC with buck).

2.2.1 *Circuit topology breakdown*

The total count and percentage breakdown of power converters implemented or simulated in the reviewed papers are shown in Table 2.1 and Fig. 2.1 in terms of major circuit topology regardless of circuit architecture details. The majority are based on the buck topology, followed by the SC in second place, whilst combinations of SC and buck topologies may have good opportunities in the near future, especially for applications where the input voltage is much higher than the output voltage. On the other hand, buck-boost, boost, Cuk and Class-E topologies are rarely investigated. Magnetics based topologies have the advantages of smooth output voltage regulation (because of its

inherent behaviour against switched voltage in voltage-driven converters) and well-established control circuits. So, they are compatible with applications requirements. SC based topologies have better power density in general because of the high energy density of capacitors. However, the output voltage is controlled based on fixed conversion ratio steps, so smooth output regulation and transient behaviour still present difficult challenges. Besides, large numbers of switches increase overall SC circuit complexity. Instead, many researchers now combine the advantages of magnetics based and SC topologies for better overall performance.

Table 2.2 and Fig. 2.2 show a more detailed breakdown of reviewed converters having more architecture complexity. Note that in Table 2.2, if the converter circuit applies to more than one category, it is added to all types that apply. Interleaving and coupled magnetics are the most investigated circuit topologies. However, some solutions combine several forms of complexity, e.g. interleaving + coupled magnetics + cascode switching.

Table 2.1 Major circuit topology breakdown.

Circuit Topology	Count	%
Buck	45	62.5%
SC	14	19.4%
SC + Buck	4	5.6%
Buck-Boost	3	4.2%
Class E	3	4.2%
Boost	1	1.4%
Cuk	1	1.4%
LLC	1	1.4%
Total	**72**	

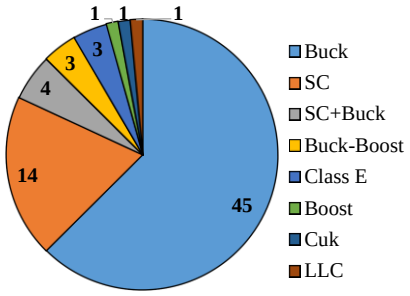


Fig. 2.1 Circuit topology breakdown.

Table 2.2 Detailed circuit topology breakdown.

Circuit Topology	Count	%
Multiphase	32	56.1%
Coupled magnetics	11	19.3%
Multioutput	8	14.0%
Resonant	5	8.8%
Cascode	1	1.8%
Total	**57**	

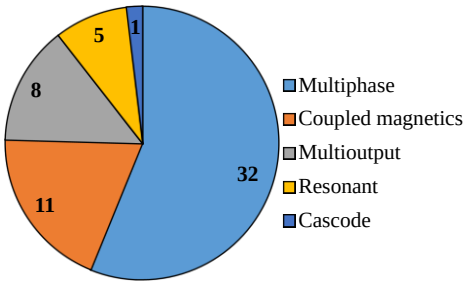


Fig. 2.2 Detailed circuit architecture breakdown.

2.2.2 *Converter peak efficiency*

In terms of circuit performance, Fig. 2.3 compares the peak efficiency versus switching frequency for the studied converters categorized based on circuit topology, with corresponding results of efficiency versus power presented in Fig. 2.4. Note that for

solutions that combine SC with the buck, the switching frequency of the buck stage is reported in the plot. The graphs show a widespread application of the buck topology. Some converters achieve peak efficiency around 90% at very high frequency 100-170 MHz [4], [17], [13], [18], at output power levels of 0.35, 4.84, 12.6, and 0.17 W, respectively.

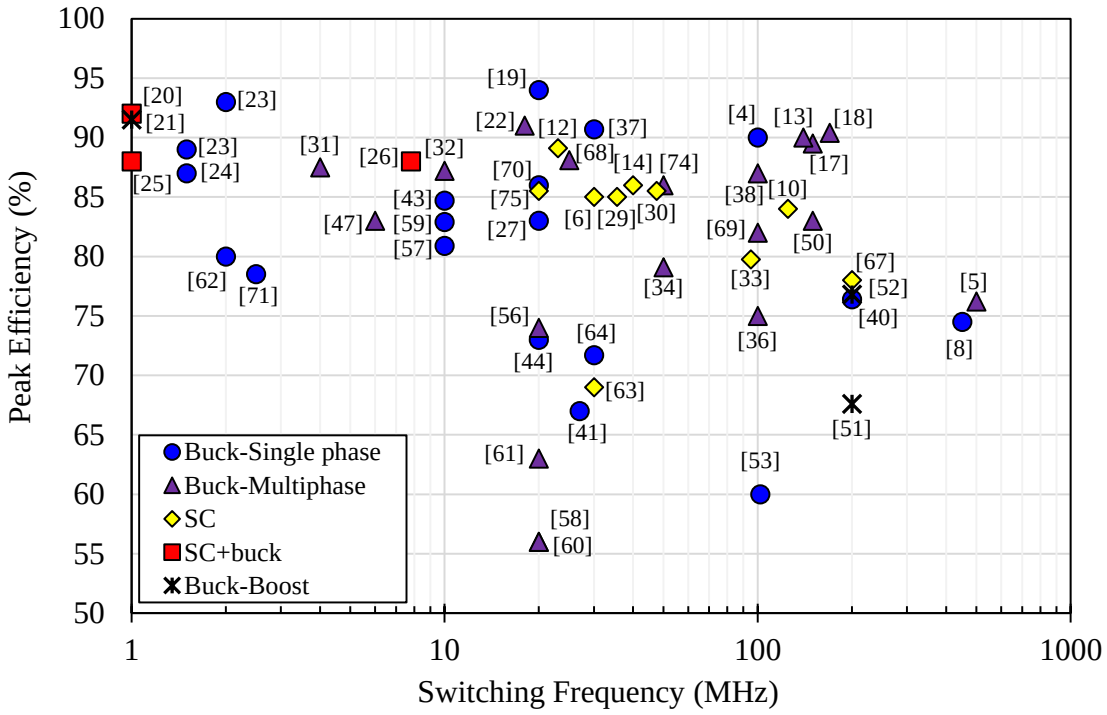


Fig. 2.3 Peak Efficiency vs. Switching Frequency.

The maximum noted efficiency above 10 MHz is 94% at 20 MHz achieved by Sepahvand et al. in [19]. This high efficiency can be explained as it used a Zero Voltage Switching (ZVS) buck topology with GaN switches and an off-chip air core 160 nH inductor to deliver 9 W power. The 6.3 W SC by Schaef and Stauth in [12] achieved 89.1% using a three-phase interleaved resonant SC topology with three 4.5 nH Through-Hole Via (THV) inductors at 23 MHz. While the highest efficiency of references shown in Fig. 2.3 was achieved with a hybrid topology (SC + Buck) was 92% at 1 MHz and 25 W, but with a 2.5 µH discrete inductor and 44 µF output capacitors (Prodic et al.) [20]. Similarly, in [21], 91.5% efficiency was predicted by Chang for a simulated dual output buck-boost converter, but at a lower power of 0.45 W with a big off-chip 10 µH inductor and 9.4 µF output capacitors. The highest frequency solution is at 500 MHz [5] for a fully on-chip two-phase buck converter with inversely coupled air-core inductors (1.54 nH each) by Lee et al.; it achieved 76.2% efficiency to deliver 0.48 W and occupies 1.56 mm^2. At a lower power density but similar frequency of 450 MHz, Tang et al. in [8] presented a

fully on-chip single-phase buck converter with a fourth-order low pass filter implemented using air core inductors (1.8 nH each); it achieved 74.5% efficiency to deliver 0.126 W, and occupies 0.65 mm^2.

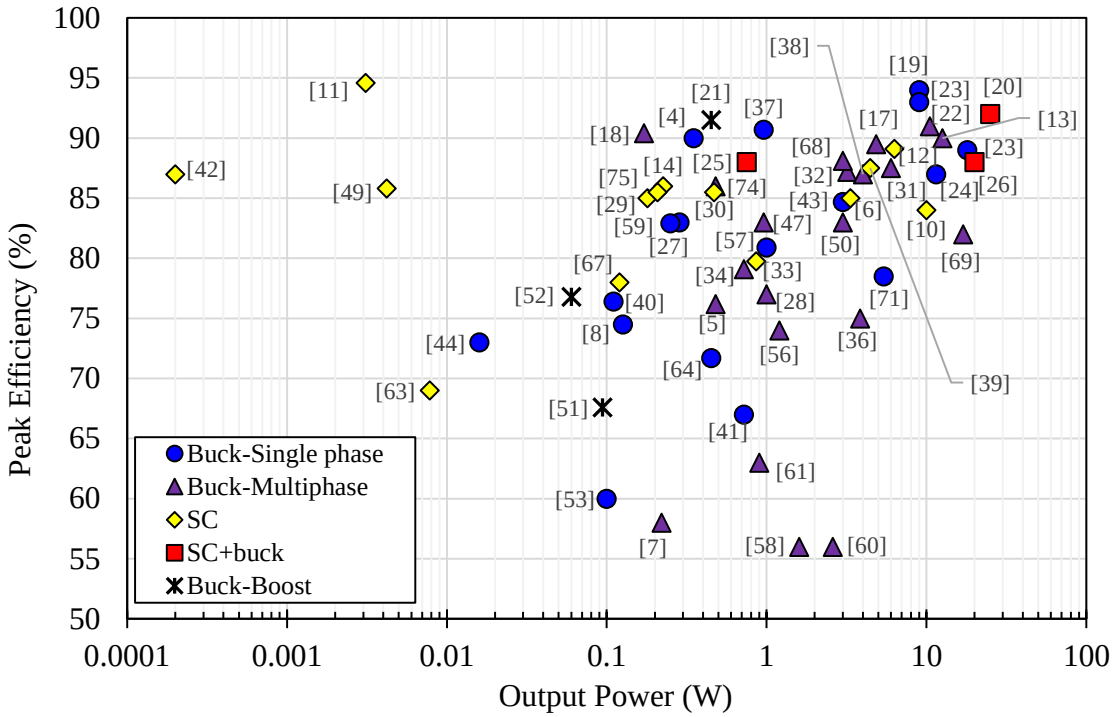


Fig. 2.4 Peak Efficiency vs. Output Power.

Converter peak efficiency versus output power in Fig. 2.4 shows that the operating range of nearly 0.1~10 W is dominated mostly by buck converters. The SC topology seems to be the main player at very low power < 10 mW, however, it is also investigated in the range 1~10 W. Around 10 W, the efficiency of buck circuits reaches 87~94% using co-packaged inductors in [13] (Intel) and [22], a PCB inductor in [23] (CPES), and discrete inductors in [19] and [24], with multiphase buck circuits performing slightly less. Meanwhile, the SC achieves similar efficiency of 89% at 6.3 W [12]. A SC and buck combination gained 88% at 0.75 W and 20 W in [25] (Prodic) and [26] (PowerChip Program), respectively, both with discrete passives. The highest power SC is the fully on-chip 64 phase converter presented by IBM in [10] which was implemented with deep trench capacitors; it reached 84% at 10 W maximum output power with a switching frequency varying from 12 to 125 MHz dependent on the load. However, it operates at two dedicated voltage conversion ratios of 3:2 & 2:1, which means a limited range of operation. Tyndall's integrated converter in [27] has a high efficiency among reviewed on-chip converters (i.e. 83%), but also with large converter footprint area (i.e. 11 mm^2) compared to other solutions. Kim et al. in [28] implemented a fully integrated 4-phase

three-level buck converter with variable switching frequency 50-200 MHz and four 1 nH inductors, reaching 77% efficiency for 1 W output power. Resonant SC converters with on-chip inductors in [29] and [30] achieved 85 and 85.5% peak efficiency.

Efficiency is plotted versus voltage conversion ratio (V_{OUT} / V_{IN}) in Fig. 2.5. Most SC converters achieved peak efficiency around a conversion ratio range of 0.3-0.5, with very few considering low and high extreme duty cycles. Instead, the combination of a SC + Buck stage by Prodic et al. in [20] and [25] achieved high efficiency at low duty cycle due to multistage voltage conversion; also, they employed large discrete inductors of 2.2 and 2.5 µH, respectively. Work in [23] and [31] was completed by the same group, where they achieved high efficiencies at low duty cycle; this can be explained by the use of GaN switches with relatively large PCB inductors having > 200 mm^2 footprint area. High efficiency at a high voltage conversion ratio of 0.75 is achieved by a ZVS buck converter in [19], i.e. 94%, which is related to employing a large off-chip 160 nH air core inductor and large 1 µF off chip output capacitor.

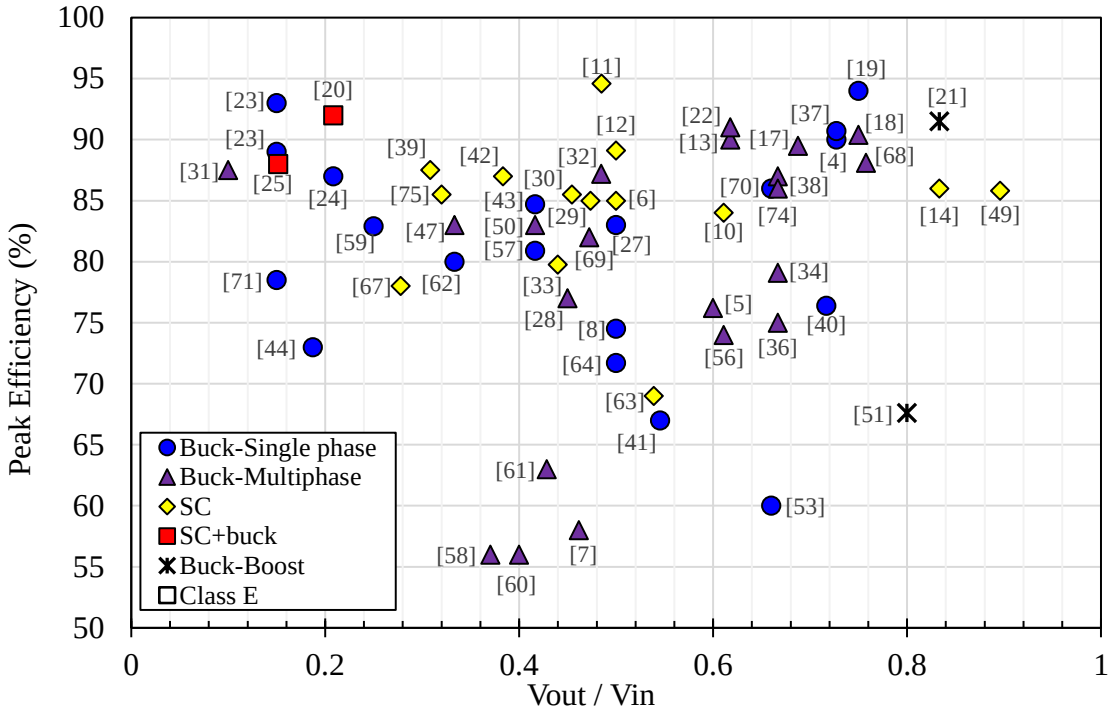


Fig. 2.5 Peak Efficiency vs. Conversion Ratio.

Power density is a critical evaluation parameter of power converters. However, for accurate evaluation, power density should be accompanied by other information like level of integration and whether the reported area is the total circuit area or only the active semiconductor area. In this case, power density is based on the total circuit area. The

number of data points is lower in this case because it is not so easy to get power density data as a common baseline because the integration level of passives, control and gate drive circuit varies from one converter to another, and the information is not always readily provided in the papers. Fig. 2.6 shows peak efficiency versus power density, where some data points are reported directly by the researchers and others are calculated from other data provided. As seen, the multiphase buck converter of Intel in [13] and IBM's multiphase SC converter in [10] are very competitive, as they achieved power densities of 2.1 and 3.2 W/mm^2 and efficiencies of 90% and 84%, respectively, for fully integrated solutions. As discussed before, the SC in [10] has the drawback of dedicated conversion ratios 3:2 and 2:1.

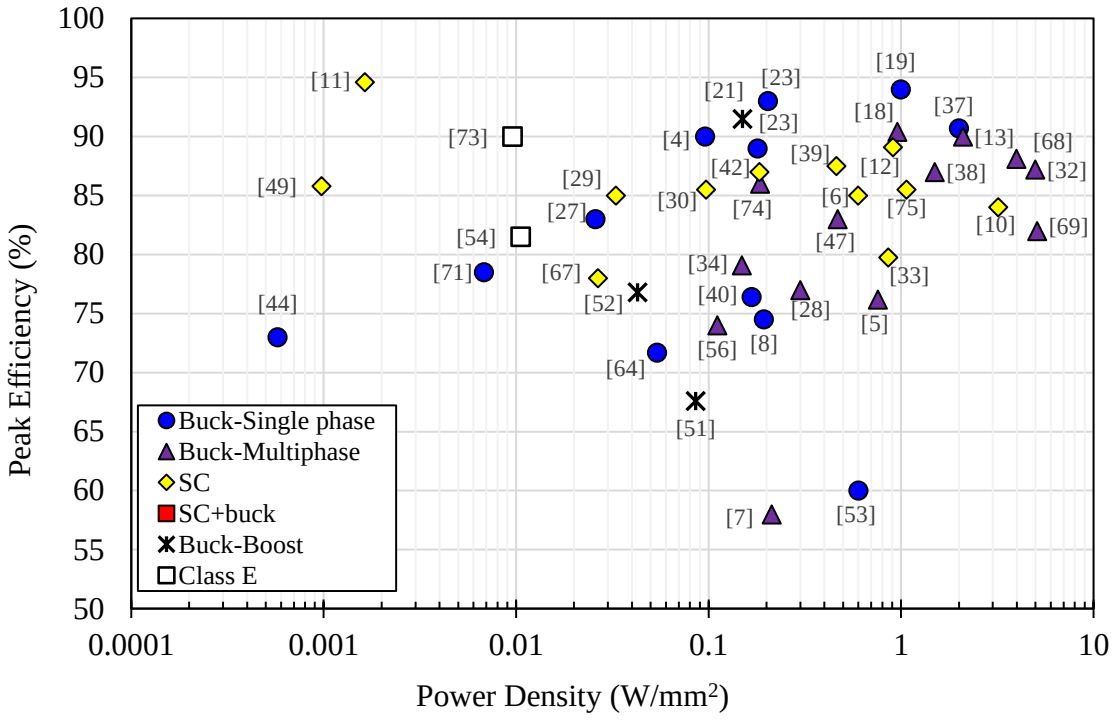


Fig. 2.6 Peak Efficiency vs. Power Density.

As for fully integrated inductor on-chip solutions; in terms of (efficiency-density) product, the highest efficiency of references shown in Fig. 2.6 was achieved by Lee et al. with a 2-phase buck converter with air-core coupled inductors (each 1.54 nH) and switching at 500 MHz [5], it achieved 76.2% efficiency and 0.76 W/mm^2 density. Also, Kim's et al. integrated converter in [28] reached a maximum power density of 0.3 W/mm^2 and 77% efficiency. Achieving high efficiency and high power density is much easier with off-chip magnetics as in [19] and [32]. As mentioned before, GaN is combined with an off-chip air core inductor in [19], while the converter in [32] is a 4-phase buck

switching at 10 MHz and employing four off-chip inductors having 1.2 µH in total and 2 µF off-chip output capacitor.

2.2.3 *Multiphase interleaving*

In terms of interleaved (multiphase) topologies, maximum power density shows a positive trend versus the number of phases in Fig. 2.7. This highlights the value of interleaving to reduce the overall converter size while maintaining high efficiency. However, multiphase converter efficiencies range between 55~95%, as shown in Fig. 2.8 without a clear trend. The interleaved SC topology is employed in [10] and [33] with 64 and 32 phases, respectively. The work of IBM in [10] is the most interesting as it achieved 3.2 W/mm^2 power density using deep trench silicon integrated capacitors, while that reported in [33] (Sanders et al.) achieved only 0.86 W/mm^2 with integrated capacitors. It should be noted that while the efficiency of the multiphase SC converter in [11] is very high, it has a low power density of 1.64 mW/mm^2.

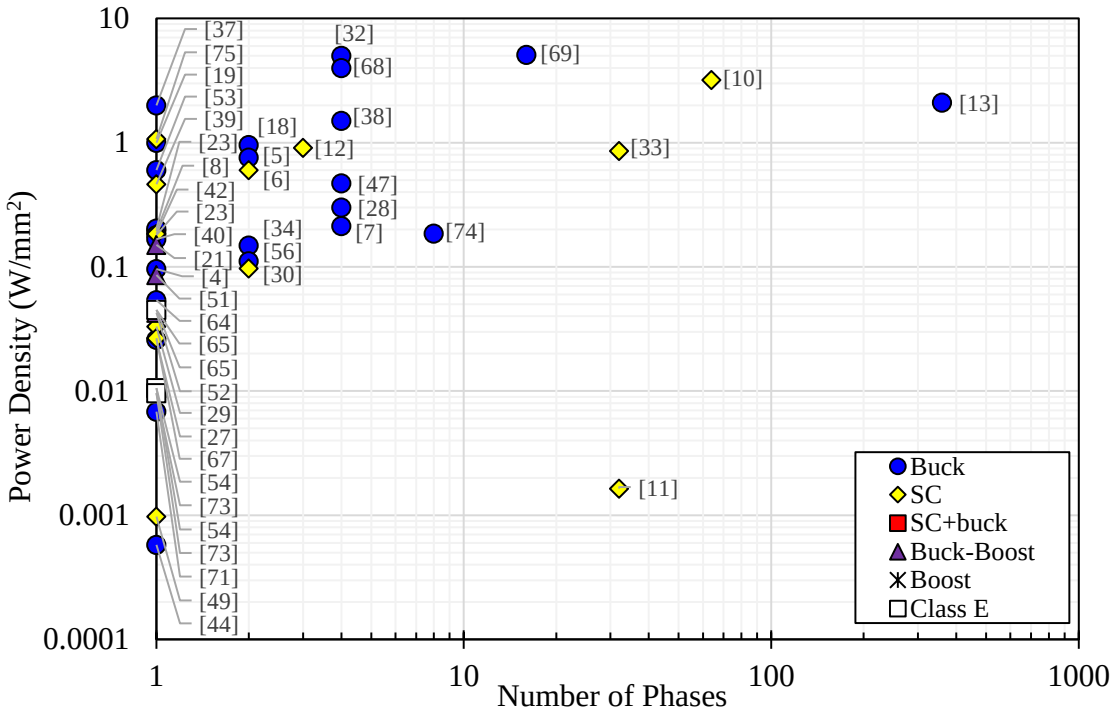


Fig. 2.7 Power Density vs. Number of Phases.

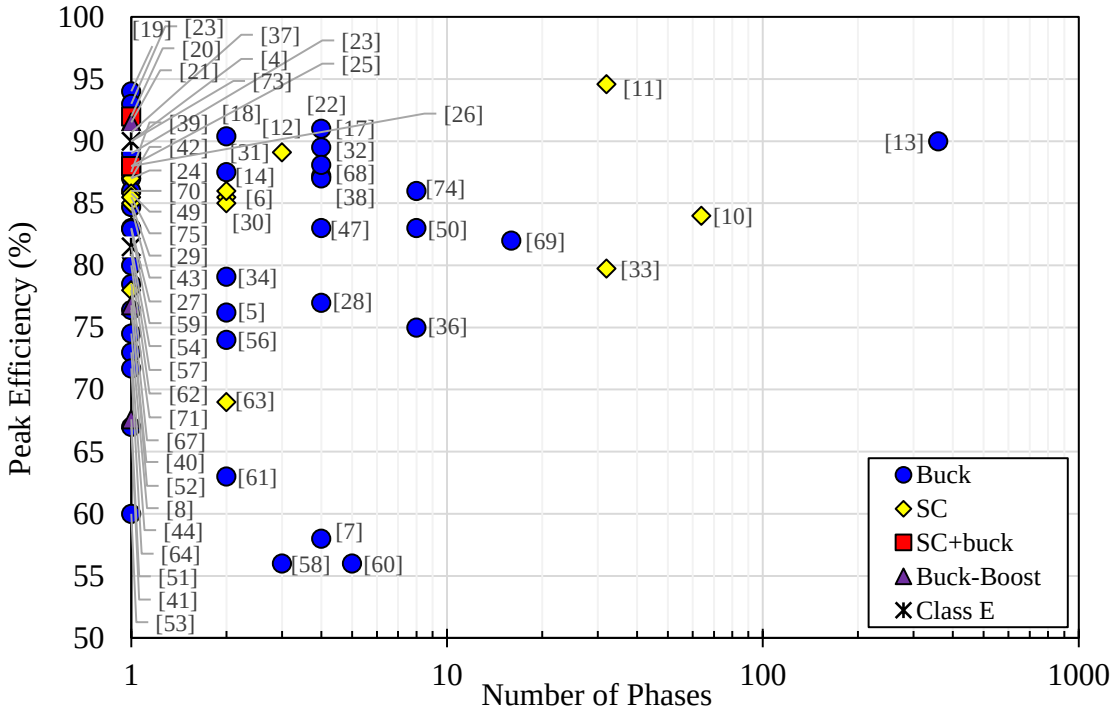


Fig. 2.8 Peak Efficiency vs. Number of Phases.

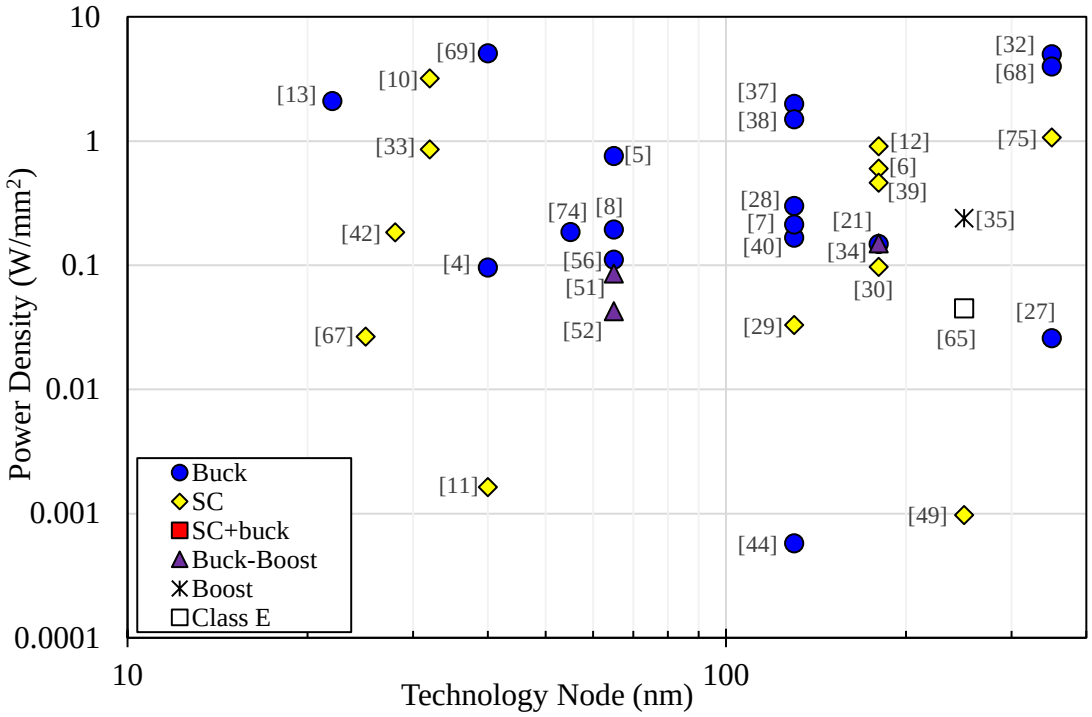


Fig. 2.9 Power Density vs. Technology node.

Fabrication technology development enables a smaller technology node which is a dual-edged sword. As a smaller node facilitates switching at higher frequencies, this means size reduction of the required passives, hence the power converter can reach a smaller form factor. On the other hand, the input voltage level is also reduced, which means that

multistage topologies are necessary for high DC-DC voltage conversion ratios. Efficiency and power density are not dependent on the switches technology node length, as seen in Fig. 2.9 and Fig. 2.10; however, it is included as a main parameter of interest for integrated power converters.

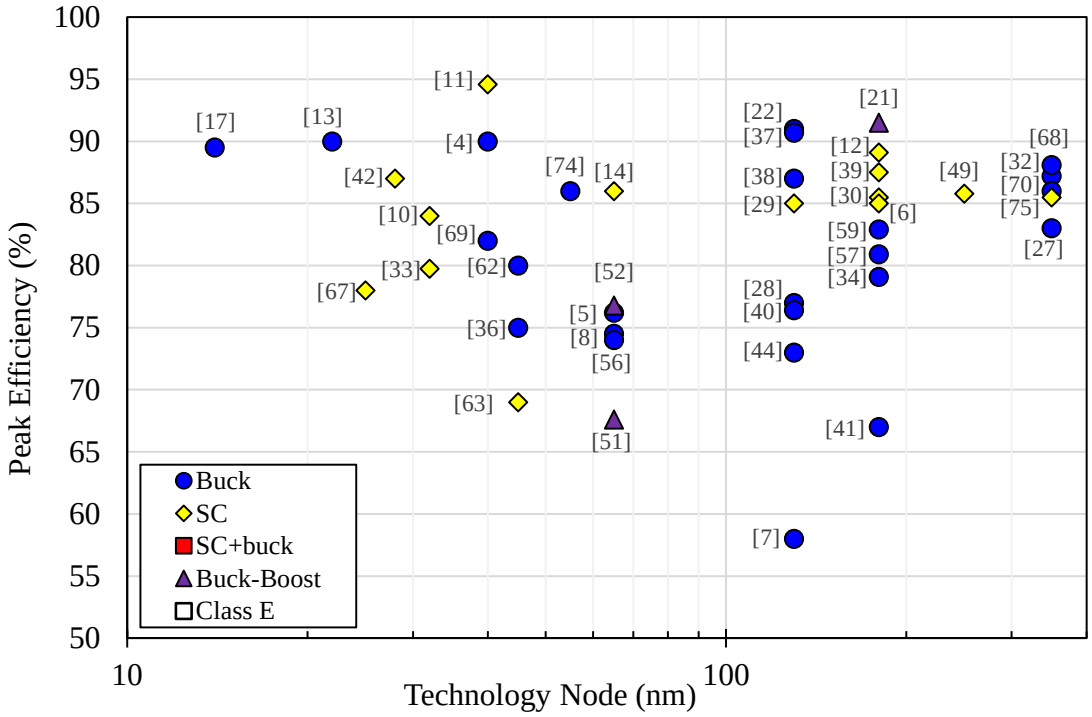


Fig. 2.10 Peak Efficiency vs. Technology node.

2.3 *Magnetics technology and integration*

Magnetic components are usually the largest and most costly components in most DC-DC converter topologies while also contributing significant losses. Their design varies based on circuit topology, e.g. single/multiple phase, flyback and resonant converters. Common types of magnetics are inductors (air core, gapped/un-gapped core), coupled inductors (positive/negative coupling) and transformers. In terms of structure, planar designs are becoming more preferred to obtain lower heights for thin profile final products. This is particularly true in the case of PwrSoC and power-supply-in-package (PwrSiP).

2.3.1 *Magnetics literature breakdown*

A breakdown of magnetic component types used across all papers reviewed is shown in Fig. 2.11 and Table 2.3, including on-chip and off-chip designs. Spiral, solenoid and racetrack are the majority planar types. Note that coupled spiral inductors are included in the "spiral" category and the same for racetrack and solenoid coupled inductors. So, the

total coupled inductor percentage 11.3% is comparable to the indicated for non-standard and unknown structures. Note that the "Unknown" category shows the proportion of papers that did not disclose magnetics data. This breakdown is regardless of integration level.

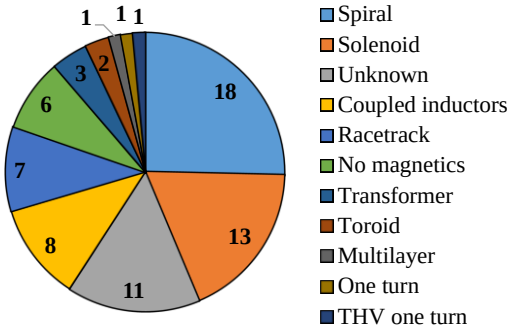


Fig. 2.11 Magnetic component type breakdown.

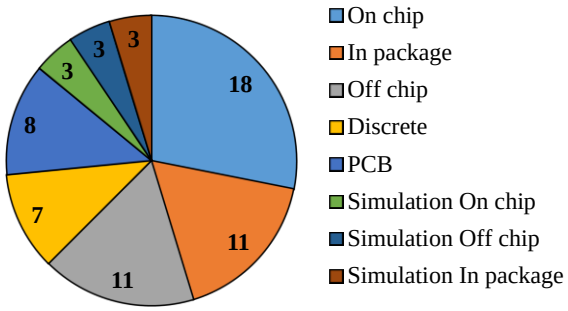


Fig. 2.12 Magnetics integration level breakdown.

Table 2.3 Magnetic component type breakdown.

Inductor Type	Count	%
Spiral	18	25.4%
Solenoid	13	18.3%
Unknown	11	15.5%
Coupled inductors	8	11.3%
Racetrack	7	9.9%
No magnetics	6	8.5%
Transformer	3	4.2%
Toroid	2	2.8%
Multilayer	1	1.4%
One turn	1	1.4%
THV one turn	1	1.4%
Total	**71**	

Table 2.4 Major circuit topology breakdown.

Inductor Integration	Count	%
On chip	18	28.1%
In package	11	17.2%
Off chip	11	17.2%
Discrete	7	10.9%
PCB	8	12.5%
Simulation On chip	3	4.7%
Simulation Off chip	3	4.7%
Simulation In package	3	4.7%
Total	**64**	

The noted information regarding magnetics integration level is shown in Fig. 2.12 and Table 2.4, where integration terms used are defined as follows:

- On-chip: inductor is integrated on silicon.
- Discrete: the entire system including inductor is discrete.
- In-package: discrete inductor is co-packaged with the IC chip in a boxed or molded package but not integrated on the same silicon die.
- Off-chip: the converter is integrated on silicon chip with an external inductor.
- PCB: inductor is fabricated on the PCB or embedded in the PCB.
- Simulation (on/off-chip, in-package): the system is simulated but with chip layout or package design presented for future fabrication.

The high interest in using integrated magnetics in high-frequency converter development and performance is evident. On-chip and in-package categories, including simulation, represent around ~50% of the reviewed papers. Also, PCB integrated inductors are of interest as they can be scaled down to fit standard encapsulated packages, e.g. MLP, QFN. Discrete systems are noted here to enable comparison in terms of their operating parameters, e.g. V_{IN}, V_{OUT}, F_{SW} and P_{OUT}.

2.3.2 *Magnetics utilization*

Fig. 2.13 shows converter power density versus total inductance categorized based on integration level and circuit topology accompanied with the number of phases shown as data labels. Total inductance is used for comparisons instead of inductance per phase, so that any other inductance in the circuit is counted for a more fair comparison. Clearly, higher power density is achieved with off-chip designs, with the advantages of interleaving showing again both for discrete [19], [32], co-packaged inductors [13] and silicon integrated parts [8].

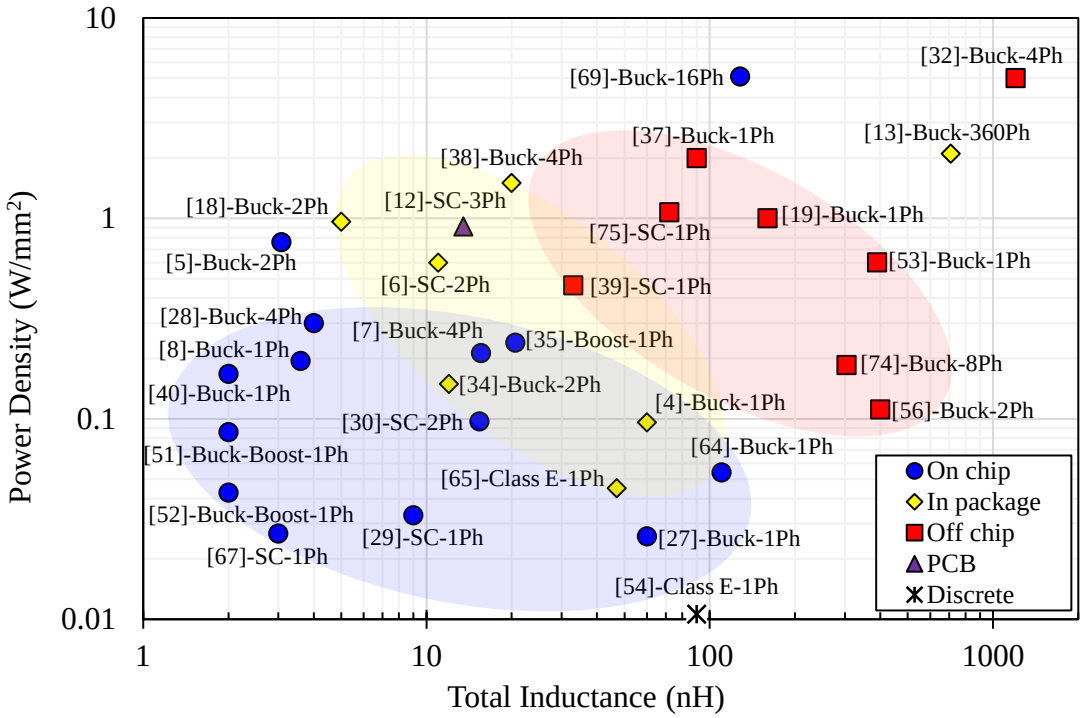


Fig. 2.13 Converter power density vs. total inductance.

Focusing only on the inductor, Fig. 2.14 shows inductor power density vs. total inductance in the converter (Inductor power density = P_{OUT} at peak efficiency / total inductor area). On average, it seems that in-package designs could achieve the highest inductor power density. However, on-chip inductors are developing as well and are not

far behind the performance of in-package inductors. Kim's fully integrated 4-phase three-level buck converter in [28] employed four spiral inductors (each 1 nH) and recorded the highest on-chip inductor power density of 1.56 W/mm^2. However, the highest in-package inductor power density reached 3.6 W/mm^2 with a 2-phase buck converter in [34]. Both Fig. 2.13 and Fig. 2.14 show that the challenging power density range is above 1 W/mm^2.

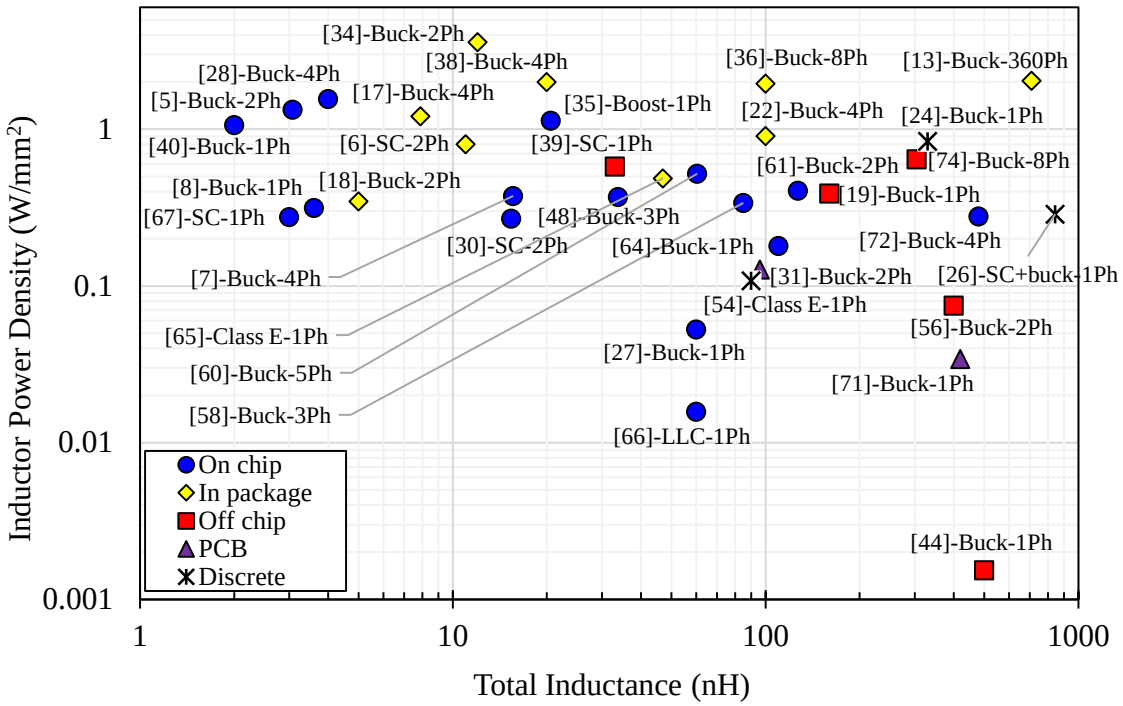


Fig. 2.14 Inductor power density vs. total inductance.

2.4 *Semiconductor technology*

It is known that MOSFET switches are usually evaluated based on total gate charge and drain to source resistance (R_{DS_ON}). However, such details are not mentioned in many of the reviewed papers, which are more focused on circuit parameters, e.g. maximum voltage, current and switching frequency, as the aim of the research is the development of circuit architecture, magnetics or control performance.

Therefore, the summary of the reported performance of semiconductor switches provided in this section focuses on their operation in high-frequency PwrSoC applications regarding switching frequency, current carrying capability and switched voltage levels. As might be expected, a significant number of papers are based on custom semiconductor switches designed for fully integrated PwrSoC solutions, with the majority being based on CMOS technology. A comparison of the range of switching frequency, current

handling capability, and switched voltage vs. technology node as applied in such demonstrator circuits is given in Fig. 2.15, Fig. 2.16, and Fig. 2.17.

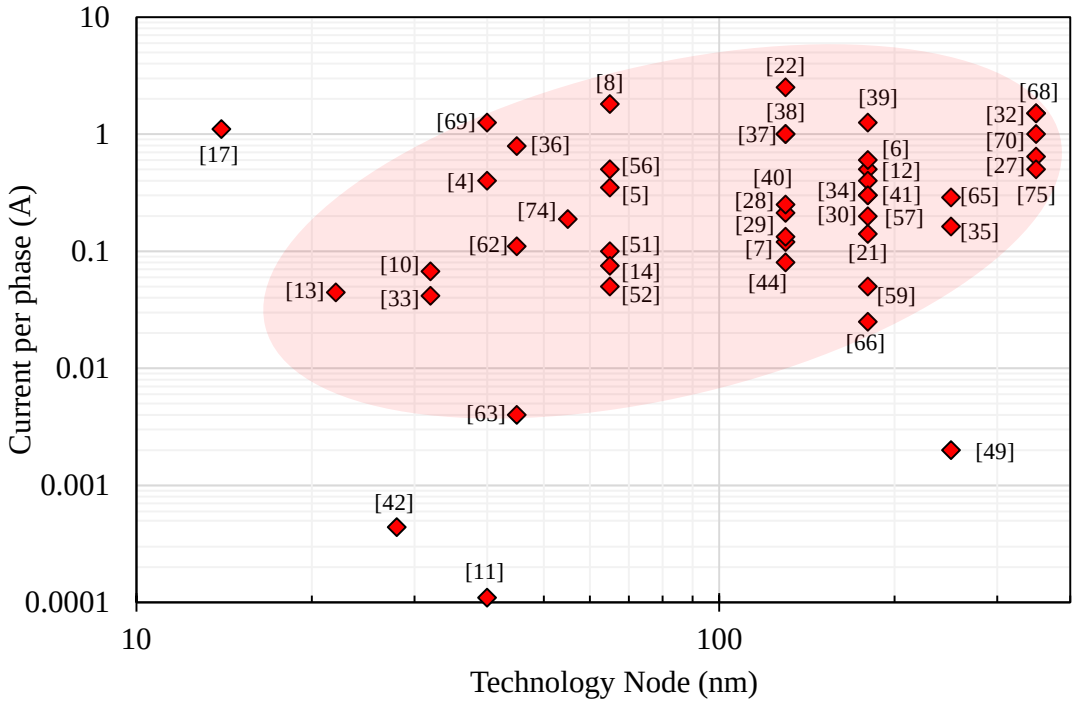


Fig. 2.15 Current per phase vs. technology node.

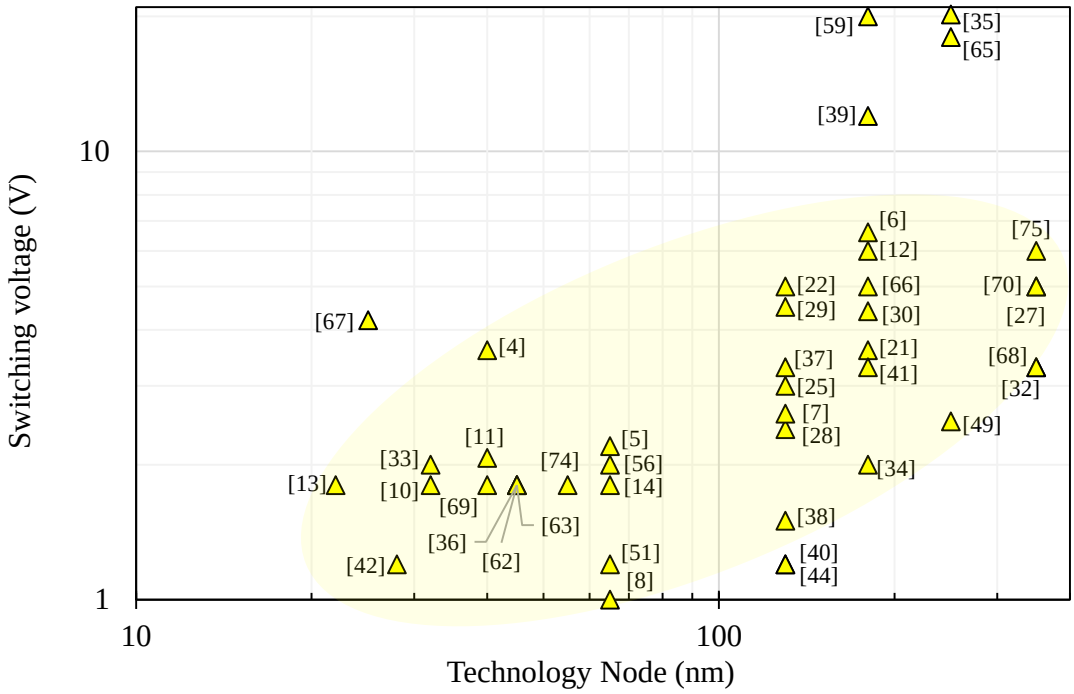


Fig. 2.16 Switching voltage vs. technology node.

Apart from one outlier point, representing the only GaN-on-Si custom solution [35] in Fig. 2.18, there is some trend of increasing switching frequency with decreasing

technology node. Clearly, frequencies of 100's MHz are supported by custom semiconductors for PwrSoC. Similarly, while the trend is not very well defined, there is some correlation between applied current/voltage levels with the technology node.

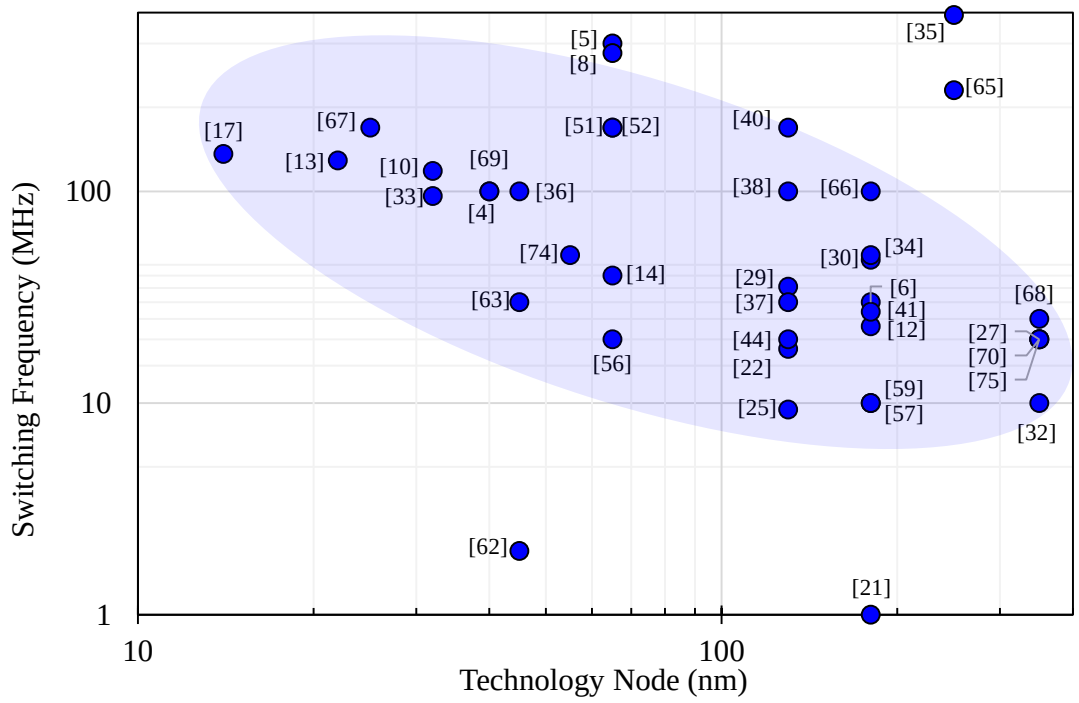


Fig. 2.17 Switching frequency vs. technology node.

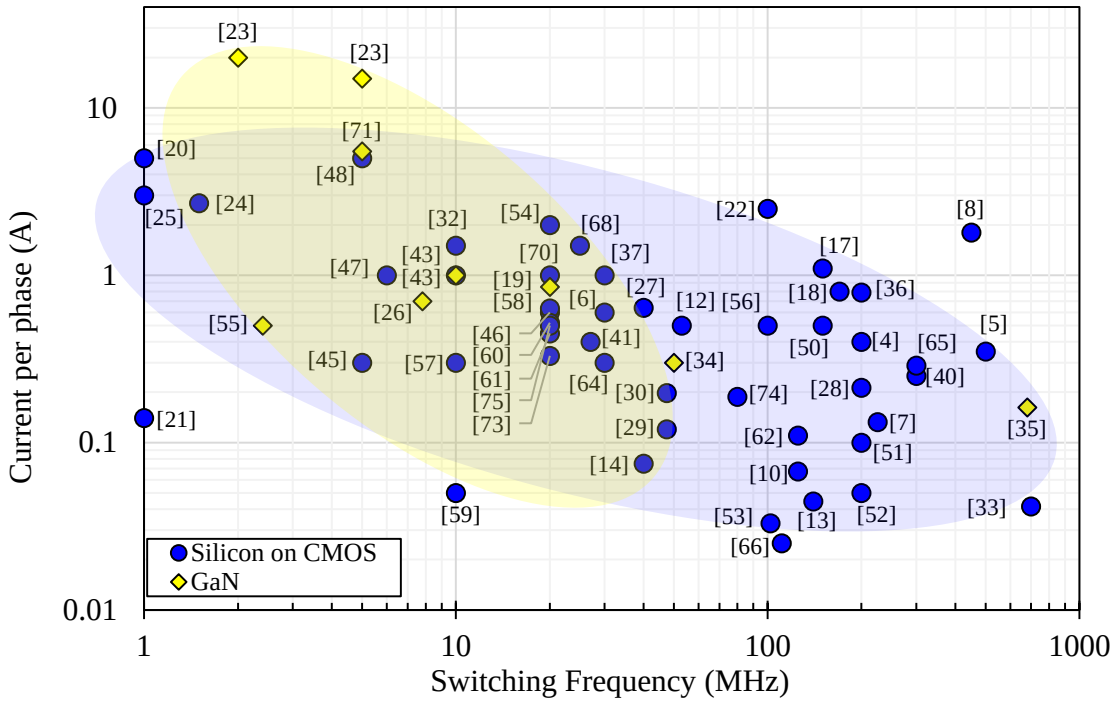


Fig. 2.18 Current per phase vs. switching frequency.

In order to investigate these relations further, the variation in current handling vs. switching frequency is presented in Fig. 2.18 where, as might be expected, it is found that there is a general, although not very well defined, inverse relationship. For frequencies higher than 10 MHz, current levels are limited to 1 A. Results in this case include all types of semiconductors reported in the literature, including discrete and fully integrated PwrSoC devices. It is found that GaN supports current levels of up to 15 A switching at 5 MHz [23], with lower current levels of the order of 160 mA supported at frequencies up to 680 MHz [35]. Similarly, for CMOS (TI NexFET, [23]), current levels of up to 20 A are supported at frequencies up to 2 MHz, while at higher frequencies, switching at 500 MHz is supported for current levels up to 350 mA with custom 65 nm CMOS [5].

Due to their ready availability, commercial semiconductors are compared separately in Table 2.5, where again, most results are based on values reported in PwrSoC solutions in the academic literature. The highest operating frequency found for a discrete silicon solution (controller + driver + semiconductors) is 20 MHz with a corresponding maximum current level of 0.65 A for the SEMTECH SC221. Higher frequency and current GaN solutions are emerging from Global Foundries, while existing products from EPC support relatively high voltage and current levels at frequencies up to 10 MHz. Sarda provides an alternative solution with GaAs switches combined with CMOS driver stages to support current levels up to 8 A at 10 MHz.

Table 2.5 Commercial Semiconductor Switches Applied in Power-Supply-on-Chip.

Manufacturer/Device		**F_{SW} (MHz)**	**V_{MAX} (V)**	**I_{OUT} (A)**
Global Foundries	PwrSoC ’16 [36] [22]	NA 10 – 100	10.5 5	0.010 – 0.040 2.5
Panasonic (GaN-GIT)	PwrSoC ’16 [36]	2	30	2
Sarda (GaAs)	PwrSoC ’16 [36]	10	12	8
Infineon	IRF8721 [20]	1	24	5
SEMTECH	SC220 [37] SC221	20 20	4.5 5.5	0.6 0.65
OnSemi	NCP6360	6	5.5	0.8
EPC (GaN)	EPC8010 [38] EPC1012 [26] EPC2007C [39]	10 7.8 2.4	24 200 45	1 3 0.5
Vishay	Si4204DY [25]	1	6.6	3
TI	NexFET [23]	2	12	20
GaN Systems	GS61004B-MR [40]	1-5	12	5.5

2.5 *Applications*

Within the scope of circuit operating parameters identified as V_{IN} (2~5 V), V_{OUT} (1~3 V), F_{SW} (10~100 MHz), I_{OUT} (1~2 A/phase), there are many applications that high-frequency PwrSoC solutions can target; including microprocessors, FPGAs, POLs, PLCs, HDDs, SSDs, laptops, mobile phones, gaming devices, wearables, cameras, camcorders, etc. The common aim between all these applications is the importance of overall solution size reduction while maintaining efficient operation. Speed of response is essential for microprocessor loads, and is therefore a primary driver for minimizing interconnect parasitic between the power supply and computing loads. Wide input voltage range industrial and automotive applications will be less interesting, with some exceptions like battery-powered subsystems and communication devices.

Peak efficiency is plotted versus output voltage in Fig. 2.19 for the range of converters considered. It shows the most targeted level range is 1~1.8 V in the first place and 2.4~5 V in the second place. This range of voltage is commonly required by low power electronic applications, e.g. mobile phones, network devices, servers, microprocessors, FPGA, etc. Interest in higher output voltage can be seen in LED driver applications as in [26]; and envelope tracking applications as in [19]. It is also noticed from the graph that multiphase buck converters are not playing far from 1 V V_{OUT}; this may mean that their loads of interest require low voltage and high currents as is typical for computing loads.

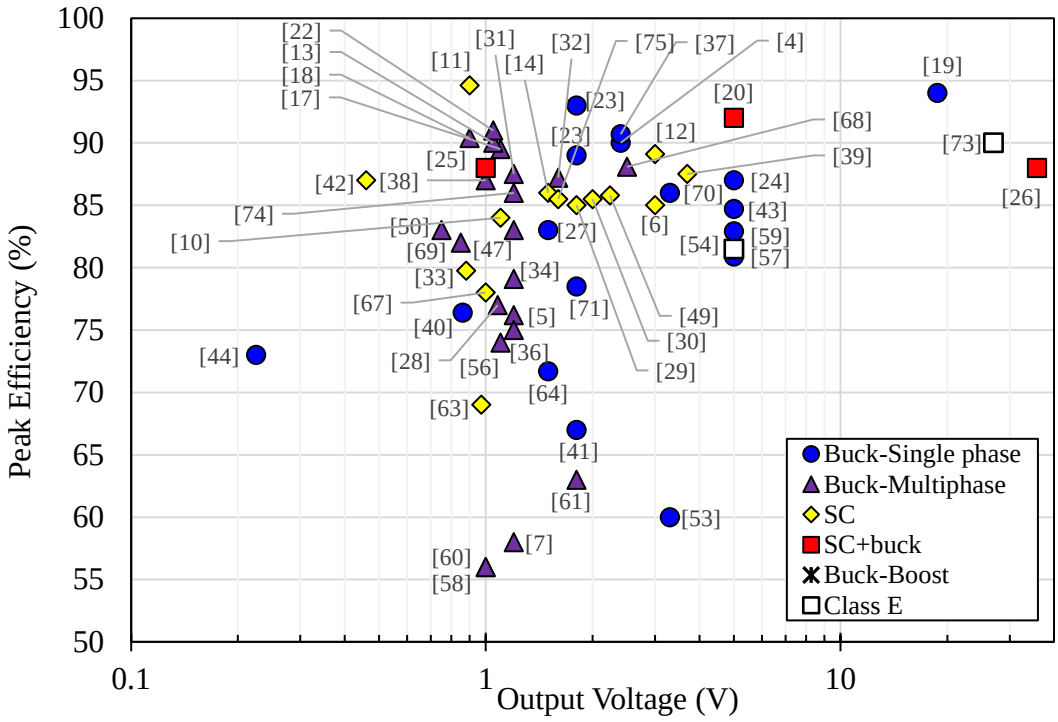


Fig. 2.19 Peak efficiency vs. output voltage.

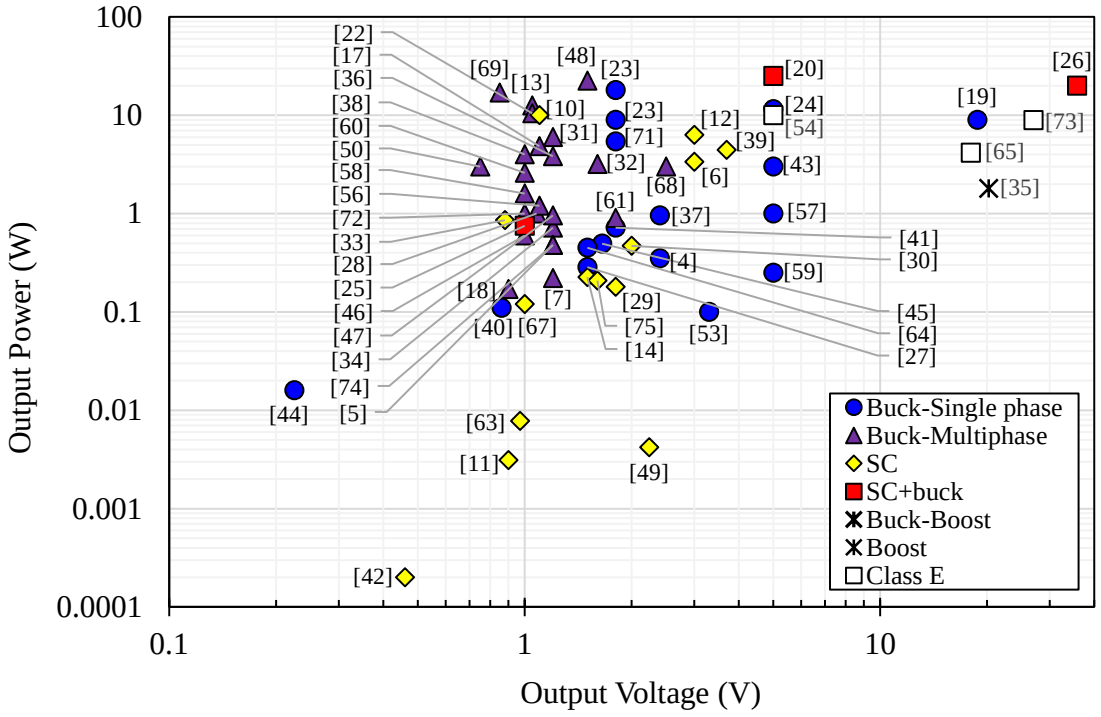


Fig. 2.20 Output power vs. output voltage.

Fig. 2.20 shows output power versus output voltage. Few reviewed papers targeted high voltage high power operation, with most applications focused on output voltages in the range of 1 – 5 V and power levels up to 25 W. The ZVS buck converter in [19] provided 9 W at up to 19 V for envelope tracking applications, with the SC + buck converter in [26] targeting LED driver applications. It is worth noting that while researchers in [26] tested a discrete converter with two 422 nH air-core inductors, they also presented a separate development on fabricated silicon embedded toroidal inductors with and without a magnetic core.

2.6 *Discussion*

This review shows a diverse comparison of performance parameters for high-frequency circuit topologies suitable for PwrSoC and PwrSiP, and the applied inductor technologies. So, it is essential to identify the most relevant work that combines the scope of the most critical performance parameters while presenting compact solutions (on-chip, in-package, PCB) within a small footprint area < 10 mm^2.

To summarize and maintain the focus on high-frequency silicon integrated inductors, papers have been filtered to include only those that have operating ranges of V_{IN} (1.5-12 V), V_{OUT} (1-3.7 V), F_{SW} (20-200 MHz), I_{OUT} (0.15-4 A), peak efficiency (>80%), node

length (40-180 nm) and total inductance (<200 nH). These are found across papers [4], [12], [28], [30], [34], [6], [41], [42], [43].

In terms of highest peak efficiency, Allard in [4] from and Cheng in [42] reached 90% and 90.7 peak efficiency with the buck topology switching at 100 and 30 MHz, respectively. In [4], a 2.5D solution for a 3-stage cascode 1-phase converter with a 60 nH co-packaged inductor was described, while [42] utilized a 90 nH off-chip inductor without disclosing its type or size. High efficiencies of 89.1% and 85% are also reported for the 3~7 W range in [12], [6] respectively, which employed a resonant SC topology using different inductor types, the most notable being a Through Hole Via (THV) in PCB by Schaef and Stauth [5].

Meanwhile, among the examined references one of the best performing fully integrated PwrSoC solutions is provided by Kim et al. [28], who employed a 4-phase three-level buck converter with variable switching frequency and achieved 77% efficiency. They used four on-chip spiral 1 nH inductors.

A fully integrated 2-phase buck converter with Glass-Substrate-Integrated Passive Device (GIPD) passives technology in [34] achieved 79.1% efficiency . In [41], Sturcken et al. applied the 8-phase buck topology with eight coupled inductors on a silicon interposer to achieve 75% efficiency at 100 MHz in a 2.5D solution.

The 4-phase Integrated voltage Regulator (IVR) in [43] achieved the highest power density of 1.5 W/mm^2 at peak efficiency of 87%; this was possible due to the small voltage conversion from 1.5 to 1 V and co-packaged on-die solenoid inductor technology.

2.7 *Summary*

It is clear that the combination of different circuit topologies provides good scope for developing more efficient power conversion for PwrSiP and PwrSoC, and that some combination of interleaved multiphase, coupled magnetics, cascode switching, SC, multistage, multiple outputs in a fully integrated system seems to be one of the most exciting areas of development for low power DC-DC conversion. Based on what has been discussed and presented throughout this chapter, it is expected that future developments on low power converters will focus on:

- Interleaved topologies for power sharing and improving light load efficiency. However, this may face limits as turning on/off phases may take longer time than the load transient requirements.
- Multilevel topologies which show capabilities for increasing power density and reduced inductor size without increasing the switching frequency. However, some challenges arise related to the gate drivers' area and losses, the ability to drive floating switches accurately, and implementation of closed loop control.
- Coupled inductors to improve load transient performance over non-coupled inductors. However, this may have challenges in terms of matching the electrical requirements and the manufactured inductor coupling factor.
- GaN technology potential in high frequency integrated converters. However, GaN FETs require a tight layout to reduce losses caused by the gate driver loop inductance, and characterisations of its dynamic on-resistance.

The next step is to investigate some of the existing solutions towards an initial demonstrator circuit design to identify the optimum combination for application of the proposed low-valued, high-frequency, integrated inductors.

Table 2.6 Summary of reviewed papers.

Ref	Year	Topology	Tech node nm	Fsw MHz	Vin V	Vo V	Io max A	Po max W	Eff max %	Area mm^2	Density W/mm^2	Magnetics	Magnetics Integration	Core	Ltotal nH	Ctotal nF
[4]	2016	Buck	40	100-200	3-3.6	1.2-2.4	0.4	0.96	90	10	0.035	Unknown	In package	-	60	49
[17]	2016	Buck	14	150	1.6	1.1	4.4	4.84	89.5	-	-	Coupled Inductor	In package	Air	7.88	-
[13]	2014	Buck	22	140	1.8	1.05	16	735	90	350	2.1	Solenoid	In package	Air	709.2	112
[18]	2020	Buck	-	170	1.2	0.9	1.6	1.44	90.4	1.5	0.96	single turn coupled	In package	Air	5	-
[19]	2016	Buck	-	20	25	6.25-18.75	0.853	16	94	16	1	Solenoid	Off chip	Air	160	1000
[12]	2015	SC	180	23-53	3.7-6	1.2-3	1.5	6.3	89.1	8.4	0.91	1 Turn THV	PCB		13.5	36.6
[20]	2017	SC+Buck	-	1	24	3.3-5	5	25	92	-	-	Unknown	Discrete	Ferrite	2500	74000
[21]	2013	Buck-Boost	180	1	1.6-3.3	2.5-3.6	0.14	0.45	91.5	3	0.150	Unknown	Off chip	-	10000	9400
[5]	2016	Buck	65	500	2-2.2	0.7-1.2	0.7	0.84	76.2	1.1	0.76	Spiral Coupled	On chip	Air	3.08	1.83
[8]	2017	Buck	65	450	0.7-1	0.5-0.8	1.8	1.44	74.5	0.65	0.194	Spiral	On chip	Air	3.6	4
[22]	2016	Buck	130	10-100	1.7-5	1-1.05	10	10.5	91	-	-	Solenoid	In package	MnZn	100	100
[23]	2014	Buck	-	2-5	12	1.8	15	27	93	132.5	0.204	Solenoid	PCB	LTCC ferrite	-	-
[23]	2014	Buck	-	1.5-2	12	1.8	20	36	89	200	0.18	Solenoid	PCB	NEC-TOKIN	-	-
[24]	2017	Buck	-	1.5	24	5	2.7	13.5	87	-	-	Coupled Inductor	Discrete	-	330	10000
[25]	2016	SC+Buck	130	9.3	3	1-2.5	-	-	-	-	-	Racetrack	In package	thin film	100	-
[25]	2016	SC+Buck	-	1	6.6	1-5	3	15	88	-	-	Unknown	Discrete	-	7100	69400
[26]	2013	SC+Buck	-	7.8	25-200	30-40	0.7	28	88	-	-	Solenoid	Discrete	Air	844	2000

[10]	2017	SC	32	12-125	1.8	0.7-1.1	4.3	10	84	4	3.2	No Magnetics	On chip	-	-	64
[27]	2013	Buck	350	20-40	2.7-5	0.5-4.5	0.64	2.88	83	11	0.026	Racetrack	On chip	-	60	-
[28]	2012	Buck	130	50-200	2.4	0.6-1.4	0.85	1	77	5	0.3	Spiral	On chip	-	4	83
[29]	2020	SC	130	35.5-47.5	3-4.5	1.5-1.8	0.12	0.216	85	7.83	0.033	Spiral	On chip	-	9	12.18
[30]	2020	SC	180	47.5	2.4-4.4	1-2.2	0.396	0.87	85.5	8.94	0.097	Spiral Coupled	On chip	-	15.4	20.8
[31]	2013	Buck	-	2-5	12	1.2	15	18	87.5	-	-	Solenoid Coupled	PCB	LTCC ferrite	96	-
[32]	2017	Buck	350	10	3.3	1.6	6	9.6	87.2	1.92	5	Unknown	Off chip		1200	2000
[33]	2011	SC	32	0.1-700	2	0.6-1.2	1.33	1.6	79.76	0.378	0.86	No Magnetics	On chip	-		-
[11]	2016	SC	40	-	1.855-2.07	0.9	0.0035	0.0031	94.6	2.44	0.00164	No Magnetics	On chip	-	-	10
[34]	2015	Buck	180	8-50	1.8-2	1.2	0.6	0.72	79.09	4.84	0.149	Spiral	In package	Air	12	15
[35]	2016	Boost	250	680	2-12	3.4-20.2	0.162	3.27	34	11	0.24	Spiral	On chip	Air	20.6	0.2
[6]	2015	SC	180	30	3.6-6.6	1.8-3.3	1.2	3.96	85	9	0.6	Solenoid	In package	Air	11	36
[41]	2013	Buck	45	125-200	1.8	0.2-1.2	6.3	7.56	75	-	-	Racetrack Coupled	In package	Thin film Ni-Fe	100	0.52
[42]	2020	Buck	130	30	3.3	1.2-2.4	1	2.4	90.7	1.2	2	Unknown	Off chip	unknown	90	940
[43]	2019	Buck	130	78-104	1.5	1	4	4	87	5.2	1.5	Solenoid	In package	-	20	200
[44]	2017	SC	180	-	12	3.5-3.8	1.25	4.625	87.5	10	0.463	Multi-layer	Off chip		33	330
[45]	2011	Buck	130	200-300	1.2	0.88	0.25	0.266	76.4	1.59	0.167	Spiral	On chip	Air	2	5
[46]	2016	Buck	180	27	3.3	1.8	0.4	0.72	67	-	-	Transformer	On chip	Co-Fe thin film	60	0
[7]	2011	Buck	130	0.75-225	2-2.6	1.1-1.5	0.53	0.8	58	3.76	0.213	Spiral	On chip	Air	15.6	12.17

[47]	2016	SC	28	-	1-1.2	0.38-0.515	-	0.0002	87	0.0104	0.184	No Magnetics	On chip	-	-	0.135
[38]	2016	Buck	-	10	12-24	5	1	21.6	84.7	-	-	Spiral	PCB	Air	18000	-
[48]	2016	Buck	130	20	0.9-1.2	0.2-0.6	0.08	0.075	73	130	0.001	Unknown	Off chip	-	500	1000
[49]	2016	Buck	-	5	3.3	1.65	0.3	0.495	-	-	-	Active inductor	-	-	5	-
[37]	2016	Buck	-	20	1.6-4.5	1	3	3	-	-	-	Coupled Inductor	Discrete	NEC flake	30	-
[50]	2015	Buck	-	6-6	3.6-4	1.2-3	4	12	83	10.24	0.47	Toroid	In package	Amorphous Fe-B-Si-C	580	-
[51]	2015	Buck	-	5	5	1.2	15	18	-	-	-	Spiral Coupled	On chip	MnZn 3F5	33.8	1E6
[52]	2014	SC	250	-	2.5	0.1-2.24	0.002	0.0042	85.8	4.3	0.001	No Magnetics	On chip	-	-	-
[53]	2014	Buck	-	150	1.8	0.75	4	3	83	-	-	Solenoid	In package	Air	-	-
[54]	2014	Buck-Boost	65	200	1	0.8-1.2	0.1	0.12	67.6	1.4	0.086	Spiral	On chip	Air	2	6.6
[55]	2013	Buck-Boost	65	200	1	1.2	0.05	0.06	76.8	1.4	0.043	Spiral	On chip	Air	2	6.6
[56]	2012	Buck	-	102	4.5-5.6	3.3	0.033	0.167	60	-	0.602	Unknown	Off chip	-	390	-
[57]	2017	Class E	-	-	-	5	2	10	81.5	945	0.011	Solenoid	Discrete	Air	90	-
[39]	2017	Cuk	-	1.8-2.4	5-45	3-50	0.5	25	93.5	-	-	Transformer	Discrete	3F46	680	9125
[58]	2016	Buck	65	20-100	1.6-2	0.6-1.2	1	1.2	74	10.8	0.111	1 Turn	Off chip	-	400	40
[59]	2016	Buck	180	10	12-48	5	0.3	1.5	80.9	-	-	Unknown	Off chip	-	500	10000
[60]	2016	Buck	-	20	2.7-3.3	1	1.9	1.9	56	-	-	Racetrack coupled	On chip	-	84.9	-
[61]	2016	Buck	180	10	20	5	0.05	0.25	82.9	-	-	Unknown	Off chip	-		-
[62]	2016	Buck	-	20	2.5-2.6	1	2.6	2.6	56	-	-	Racetrack coupled	On chip	Ni-Fe	60.5	-
[63]	2015	Buck	-	20	4.2	1.8	0.9	1.62	63	-	-	Racetrack coupled	On chip	Ni-Fe	127	-
[64]	2014	Buck	45	2-125	1.8	0.6-1.6	0.11	0.176	80	-	-	Unknown	Off chip	-	-	12.5
[65]	2010	SC	45	30	1.8	0.77-1	0.008	0.008	69	-	-	No Magnetics	On chip	-	-	-

[66]	2010	Buck	-	30	3	1.5	0.3	0.45	71.7	8.33	0.054	Racetrack	On chip	-	110	-
[67]	2018	Class E	250	300	4-12	5.5-18	0.288	4.16	47.3	0.9212	0.045	Spiral	In package	Air	47	11.05
[68]	2019	LLC	180	100-111	3-5	0.3-2	0.025	0.05	7	9.1	0.0055	Transformer	On chip	Air	60	-
[69]	2019	SC	25	200	2.8-4.2	0.6-1.2		0.04	78	1.5	26.7	Spiral	On chip	Air	3	55
[70]	2019	Buck	350	25	3.3	0.3-2.5	6	0.75	88.1	1.88	3.98	Unknown	-	-	800	2470
[71]	2019	Buck	40	100	1.8	0.85	20	17	82	3.33	5.1	Stripline	On chip	CZTB	128	56
[72]	2019	Buck	350	16-20	5	3.3	1	3.3	86	47	0.07	Spiral	PCB	unknown	150	2400
[40]	2020	Buck	-	1-5	12	1.8	5.5	9.9	78.5	1451.61	0.00682	Spiral	PCB	Air	419.7	-
[73]	2020	Buck	300E3	-	3.6	1	1	1	-	-	-	Solenoid	On chip	Thin film Co	480	-
[14]	2020	SC	65	40	1.8	0.3-1.6	0.15	0.24	86	2.91	0.0825	Unknown	Off chip	-	1000	10.6
[74]	2020	Class E	-	20	12	27	0.33	8.91	90	936.9	0.009606	Spiral	PCB	Air	166	28200
[75]	2020	Buck	55	30-80	1.8	0.6-1.2	1.5	1.8	86	9.72	0.1852	Solenoid	Off chip	thin film	304	10
[15]	2020	Buck	-	10	48	1	-	-	-	-	-	Toroid	package embedded	HPE1, RM4A	374	-
[76]	2021	SC	350	20	3-6	0.4-1.6	0.5	0.8	85.5	0.75	1.07	Unknown	Off chip	Core	72	2300

Chapter 3 – Multiphase Buck Topology

This chapter presents an analysis of low-power, multiphase interleaved buck converters to illustrate the extent to which adding more phases is beneficial for reducing the passive components' sizes. The analysis considers commercial converter specifications, i.e. input voltage range, output voltage ripple and load transient capability, and it is verified for PCB integrated inductors, thereby also accounting for the impact of PCB design rules on inductor implementation. The chapter assesses the benefit of inductor coupling, and presents guidelines for coupling factor selection to avoid steady-state inductance roll-off for a wide input voltage range. For a 5.4 W, 20 MHz converter, it is shown that by restricting the phase current ripple, the theoretical reduction in total inductor peak energy predicted for increased phase numbers is limited. In this case, the air-core PCB solenoid designs show that the total inductance density does not improve beyond 2-phases. For verification, solenoid and spiral inductors are implemented in both single- and 2-phase buck converters. When compared with single phase designs, 2-phase spiral inductors are 44% smaller and, the 2-phase solenoid has 54% lower loss. The prototype converter has a peak efficiency of almost 90% at V_{IN} = 4.5 V, V_{OUT} = 1.8 V and F_{SW} = 20 MHz.

3.1 *Introduction*

Higher power densities and the longer battery lifetimes desired for computational and battery-powered consumer products increase the motivation for smaller and more efficient devices. High-performance microprocessors, Graphical Processing Units (GPU) and other applications are powered by multiphase interleaved buck converters for DC voltage step-down requirements. Generally, the multiphase topology shown in Fig. 3.1 is a good solution for improving light-load converter efficiency, where phases can be switched off as required to reduce per-phase quiescent power loss, [13][17]. Furthermore, multi-MHz switching enables size reduction in the required passive components, particularly important for the inductors, as they are usually the biggest components in converters. Another advantage of interleaving is the partial cancellation of output current ripple and the multiplied output ripple frequency, both of which can contribute to the overall size reduction of the required passive elements for given output voltage ripple and converter transient response [5][77].

Determining the number of phases for optimized overall inductor density is essential, especially for size sensitive applications such as converters employing on-chip and co-

packaged inductors, as in [73] (1-4 phases), [75] (1-8 phases), [43] (1-4 phases), [71] (16 phases). The interleaved buck has been widely investigated for various converter specifications and packaging technologies, e.g. [7], [34], [37], [53], [70], [78]. However, to the best of the authors' knowledge, the effect of adding more phases on the overall size of the passive components while considering practical limitations, such as the effect of wide input voltage range and limited current per phase, has not been addressed.

Some attempts have been made to determine the optimum number of phases, as in [22], which evaluated the converter efficiency assuming a fixed total inductance divided equally between all phases. For silicon integrated solenoid inductors, the authors concluded that 4-phases achieved the best overall efficiency for the three converter specifications considered. However, they did not consider a wide input voltage range; besides, the basis of inductance selection may result in different total output current ripples and is therefore not a like-for-like comparison.

The variation in optimum number of phases in the previous literature is due to different application requirements and inductor technologies. This chapter addresses this deficiency by creating a design procedure to determine the optimum number of phases in terms of the overall output filter size.

Another aspect of the interleaved buck topology centers on the benefits of negative magnetic coupling between phases. Negative coupling partially cancels the DC magnetic field component, alleviating the magnetic core's saturation limit and potentially improving load transient performance. Coupled vs non-coupled inductors have been compared for various applications in [79], [80] at 300 kHz, [81] at 600 kHz, and [82] at 250 kHz, while coupled inductors have been implemented in several multi-MHz converters, e.g. [5], [18], [30], [41], [62], [83]. However, most authors consider a single input voltage value; the optimum choice of coupling factor for a wide input voltage range has not been clearly described. Therefore, this chapter analyses the coupling factor that maximizes the effective inductance per phase while also identifying the input voltage range for effective coupling.

To illustrate the findings, PCB air-core inductor designs are considered for a nominal conversion specification of 4.5 V to 1.8 V at 5.4 W. An input voltage range of 2.5-6.6 V is assumed to align with a typical battery powered converter specification. This incorporates the effect of PCB processes on inductor designs. This chapter builds on the

concepts presented in [84] but covers a broader range of applications through normalized analysis and considers air-core PCB inductors which were available for fast prototyping.

The remainder of this chapter is structured as follows. Section 3.2 presents a normalized analysis of the multiphase interleaved buck converter considering practical circuit specifications and limitations. Section 3.3 presents a comparison of passive component specifications for different numbers of phases in a multiphase buck converter for a given converter specification. Section 3.4 presents the inductor modelling and design procedure applied for air-core spiral and solenoid inductors based on given PCB manufacturing design rules. Section 3.5 presents a comparison of circuit simulation and measurement results which confirm the findings on the optimum inductor designs for the fabricated inductors. Conclusions are presented in Section 3.6.

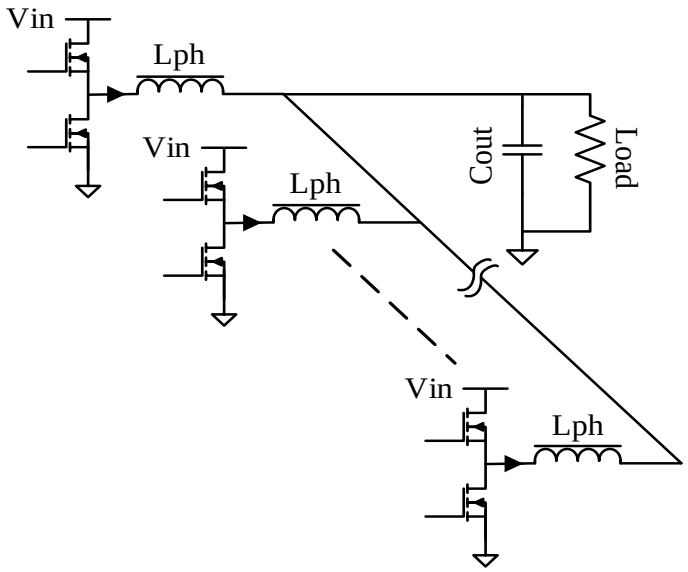


Fig. 3.1 Schematic of multiphase buck converter.

3.2 *Multiphase Interleaved Buck Analysis*

In a multiphase interleaved buck converter, each phase is shifted by 360°/N_{Ph} from the next one, where N_{Ph} is the number of phases. This interleaved operation partially cancels the overall current ripple when the phase currents are combined, resulting in smaller output ripple amplitude and multiplied frequency than non-interleaved operation. The overall output current ripple, ΔI_{Nph}, produced by the sum of phase currents is governed by the ripple reduction effect presented in [80], i.e.:

$$\Delta I_{Nph\_norm} = \frac{\Delta I_{Nph}}{\Delta I_{Ph}} = \frac{N_{Ph}}{D(1-D)}\left(D - \frac{m}{N_{Ph}}\right)\left(\frac{1+m}{N_{Ph}} - D\right) \tag{3.1}$$

where ΔI_{Nph_norm} is the normalized value of the overall output current ripple relative to the per-phase inductor current ripple, ΔI_{Ph}. D is the switching duty cycle (3.2), and m is the integer number less than or equal to $(N_{Ph}D)$ as explained in [80].

$$D = \frac{V_{OUT}}{V_{IN}} \tag{3.2}$$

Ideally, the optimum number of phases is at multiples of $(1/D)$ where, as shown by (3.1), the sum of the phase current ripples is theoretically zero. However, considering the practical requirements of individual component specifications (such as the inductors) and operation over a range of D may change the benefits of adding more phases. This work aims to find an optimum number of phases for practical converter specifications from a passive components size perspective.

3.2.1 *Inductance Selection for Multiphase Buck Converter*

As discussed in [84], inductance in a multiphase interleaved buck converter is selected to satisfy a certain total output current ripple requirement ΔI_{Nph}. In this analysis, for comparison purposes, ΔI_{Nph} is set equal to the inductor current ripple in a corresponding 1-phase converter, ΔI_{1ph}. So, the ripple reduction function in (3.1) is used to calculate the maximum allowed inductor current ripple per phase ΔI_{Ph} (3.3).

$$\Delta I_{Ph} = \frac{\Delta I_{Nph}}{\Delta I_{Nph\_norm}} \tag{3.3}$$

$$\Delta I_{Ph\%} = \frac{\Delta I_{Ph} N_{Ph}}{I_{DC}} \tag{3.4}$$

Depending on the level of ripple cancellation, (3.1)-(3.3) may predict very high values of ΔI_{Ph}. However, practically, it needs to be limited to avoid excessive current in each phase inductor. For illustration, resulting values of unrestricted and restricted $\Delta I_{Ph\%}$ (3.4) versus duty cycle are compared in Fig. 3.2(a) for a 3-phase interleaved buck converter at an overall current ripple level, $\Delta I_{Nph\%} = \Delta I_{Nph}/I_{DC} = 25\%$ at different ripple restriction conditions (100, 200 and 300%). Clearly, the unrestricted $\Delta I_{Ph\%}$ becomes very high close to theoretical optimum ripple cancellation conditions, i.e. when N_{Ph} equals multiples of $1/D$. Then phase inductance L_{Ph} is calculated as:

$$L_{Ph} = \frac{D(V_{IN} - V_{OUT})}{\Delta I_{Ph} F_{SW}} \tag{3.5}$$

where V_{IN}, V_{OUT}, F_{SW} are the specified input voltage, output voltage, and switching frequency, respectively, and ΔI_{Ph} is calculated from (3.1)-(3.3) based on N_{Ph} and the specified ripple of the summed phases current ΔI_{Nph}. This interleaving ripple reduction results in a normalized total inductance of:

$$L_{Tot\_norm} = \frac{N_{Ph} L_{ph}}{L_{1Ph}} = \frac{N_{Ph} \Delta I_{1ph}}{\Delta I_{Ph}} = \frac{{N_{Ph}}^2 \Delta I_{1ph\%}}{\Delta I_{Ph\%}} \tag{3.6}$$

relative to a single-phase converter inductance, L_{1ph}.

With the previously mentioned assumptions, L_{Tot_norm} is plotted in Fig. 3.2(b) for 2, 3 and 4 phases, dashed and solid lines are the calculated values with $\Delta I_{Ph\%}$ unrestricted and restricted at 200%, respectively. The effect of different levels of restriction are considered later. As a result of restriction, L_{Tot_norm} is clamped to a certain minimum value for an increasing duty cycle range as the number of phases increases. For example, L_{Tot_norm} for 2, 3 & 4 phases are restricted at a minimum of 50, 112.5 & 200 % respectively. For reference, the duty cycle range corresponding to V_{IN} = 2.5 ~ 6.6 V and V_{OUT} = 1.8 V is shaded in Fig. 3.2(b). This restriction also affects RMS and peak phase currents, as considered in section 3.2.2.

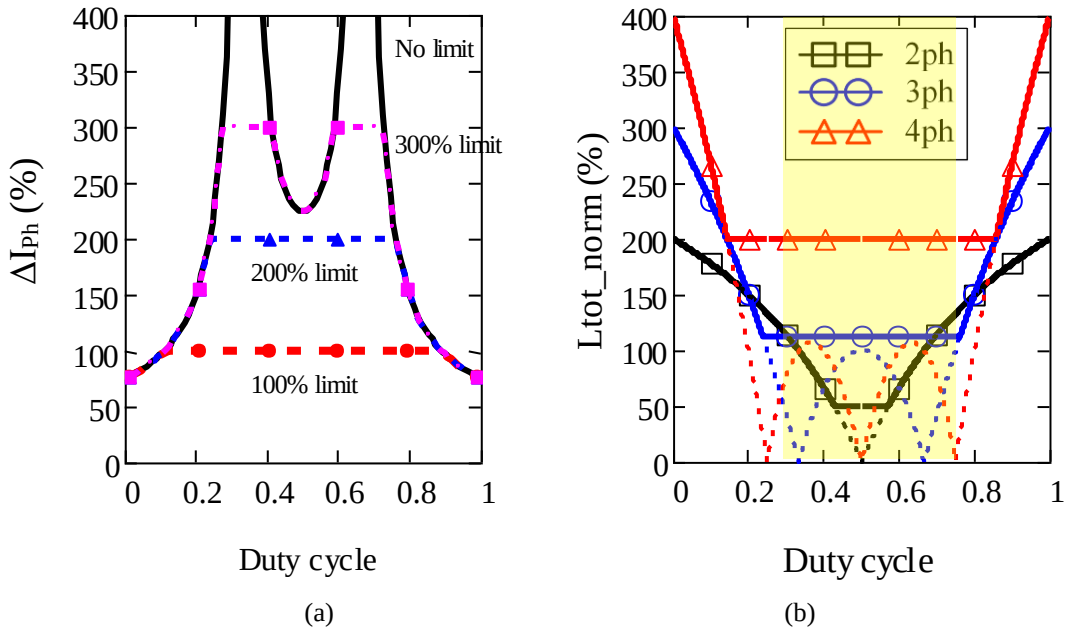


Fig. 3.2 Inductor analysis at ΔI_{Nph} = 25%: (a) 3-Phase normalised phase current ripple $\Delta I_{Ph\%}$ at different restriction conditions. (b) L_{Tot_norm}, solid and dashed lines are with $\Delta I_{Ph\%}$ restricted at 200% and unrestricted, respectively

3.2.2 *Inductor Peak Energy*

Peak energy stored in an inductor is an indicator of the inductor size. As the practical inductor in a DC-DC converter is usually required to handle the worst case of operation, i.e. at peak operating current (peak flux density), the total inductor peak energy specification is found as:

$$E_{L\_PK} = \frac{1}{2} N_{Ph} L_{Ph} {I_{Ph\_PK}}^2 \tag{3.7}$$

where I_{Ph_PK} is the phase current peak value; for a triangular current waveform, it is calculated as:

$$I_{Ph\_PK} = \frac{I_{DC}}{N_{Ph}}\left(1 + \frac{\Delta I_{Ph\%}}{2}\right) \tag{3.8}$$

For normalized analysis, I_{Ph_PK} is normalized to a 1-phase converter as:

$$I_{Ph\_PK\_norm} = \frac{I_{Ph\_PK}}{I_{1Ph\_PK}} = \frac{2 + \Delta I_{Ph\%}}{N_{Ph}(2 + \Delta I_{Nph\%})} \tag{3.9}$$

Combining L_{Tot_norm} in (3.6) and $I_{Ph\_PK\_norm}$ in (3.9), total inductor normalized peak energy is calculated as:

$$E_{L\_PK\_norm} = L_{Tot\_norm} I_{Ph\_PK\_norm}{}^{2} \tag{3.10}$$

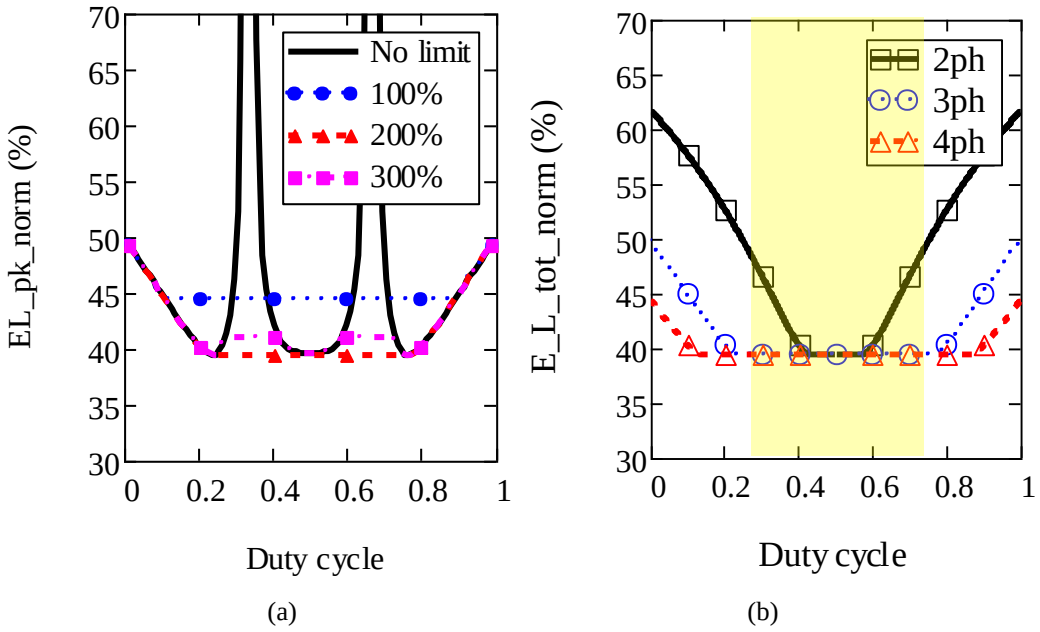


Fig. 3.3 Inductor analysis at ΔI_{Nph} = 25%: (a) 3-phase $E_{L\_PK\_norm}$ at different restriction conditions on ΔI_{Ph} showing 200% limit energy at minimum for the broadest duty cycle range. (b) $E_{L\_PK\_norm}$ with $\Delta I_{Ph\%}$ restricted at 200%.

The effect of restricted ripple current per phase on total inductor peak energy is illustrated in Fig. 3.3(a), where values of unrestricted and restricted total energy are compared for a 3-phase interleaved buck with $\Delta I_{Nph\%}$ = 25% as before. It is seen that the minimum peak energy is achieved with $I_{Ph\%}$ restricted to 200%, showing an optimum trade-off between ripple current and inductance. Similar results were found for other values of N_{ph}. Therefore 200% restricted ripple current is considered for the remainder of the paper. Graphs in Fig. 3.3(b) compare $E_{L\_PK\_norm}$ for 2, 3 and 4 phases with $\Delta I_{Nph\%}$ = 25% and 200% restriction. This comparison highlights a few main points:

- Limiting the maximum ΔI_{Ph} to 200% limits the reduction in E_{L_PK} to a minimum of 40% approximately.
- Depending on the duty cycle range, increasing N_{Ph} is not necessarily beneficial for inductor peak energy reduction and, therefore, inductor size reduction.

3.2.3 *Output Capacitance Selection for Multiphase Buck Converter*

This study assumes an ideal output capacitance to facilitate the derivation of normalized formulas to evaluate the interleaving effect on the output capacitance. A single output capacitance can be chosen to limit the steady-state output voltage ripple, ΔV_{OUT}, to a certain requirement. In the multiphase interleaved buck converter, steady-state output capacitance C_{Out_SS} is given by:

$$C_{Out\_SS} = \frac{\Delta I_{Nph}}{8 N_{Ph} F_{Sw} \Delta V_{Out}} \tag{3.11}$$

Using (3.1) and (3.6), C_{Out_SS} for N_{Ph} is normalized relative to a 1-phase converter:

$$C_{Out\_SS\_norm} = \frac{C_{Out\_SS\_Nph}}{C_{Out\_SS\_1ph}} = \frac{\Delta I_{Nph}}{N_{Ph} \Delta I_{1ph}} = \frac{\Delta I_{Nph\_norm} \Delta I_{Ph\%}}{{N_{Ph}}^2 \Delta I_{1ph\%}} \tag{3.12}$$

$C_{Out\_SS\_norm}$ in (3.12) is plotted in Fig. 3.4(a) for 2, 3 and 4 phases at $\Delta I_{Nph\%}$ = 25%. The graph shows that as long as $\Delta I_{Nph\%} = \Delta I_{1ph\%}$, then $C_{Out\_SS\_norm} = \frac{1}{N_{Ph}}$ as a result of frequency multiplication. However, when $\Delta I_{Ph\%}$ is limited to 200%, ripple cancellation may result in a further reduction in the C_{Out_SS} value as the phase inductance is increased in this region.

Another perspective of output capacitance selection is to fulfill the load transient requirement. For a buck converter with D < 0.5, the transition from high current, I_{High}, to a lower level, I_{Low}, results in the largest voltage deviation, where the output voltage overshoots by V_{OS} while the inductor discharges (and vice versa for the transition from I_{Low} to I_{High}). So, the output capacitance may be selected to compensate for the change in inductor energy [85]. Note that considering the controller delay to respond to load change may result in the opposite, i.e. $V_{US} > V_{OS}$; however, this is not the scope of this study. In the multiphase buck and assuming an ideal controller, the output capacitance for load transient requirement C_{Out_Tr} can be calculated as:

$$C_{Out\_Tr} = \frac{L_{Ph}\left({I_{High}}^2 - {I_{Low}}^2\right)}{2 N_{Ph} V_{OS} V_{Out}} \tag{3.13}$$

Then C_{Out_Tr} is normalized to the capacitance of a 1-phase converter as:

$$C_{Out\_Tr\_norm} = \frac{C_{Out\_Tr\_Nph}}{C_{Out\_Tr\_1ph}} = \frac{L_{Ph}}{N_{Ph}L_{1ph}} = \frac{L_{Tot\_norm}}{{N_{Ph}}^2} \tag{3.14}$$

$C_{Out\_Tr\_norm}$ in (3.14) is plotted in Fig. 3.4(b) for 2, 3 and 4 phases at $\Delta I_{Nph\%}$ = 25%. Comparison between Fig. 3.4(a) and (b) shows that limiting $\Delta I_{ph\%}$ affects $C_{Out\_Tr\_norm}$ differently to $C_{Out\_SS\_norm}$. However, understanding of C_{Out_Tr} selection is more important as it is practically much larger than C_{Out_SS}.

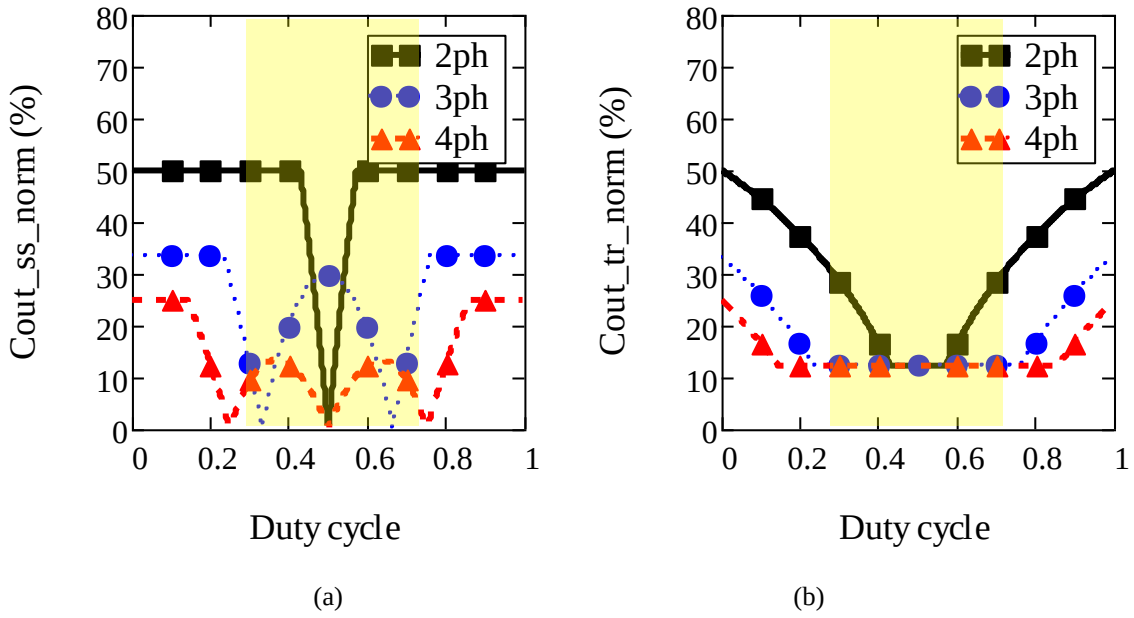


Fig. 3.4 Output capacitor analysis at ΔI_{Nph} = 25%: (a) $C_{Out\_SS\_norm}$, (b) $C_{Out\_Tr\_norm}$.

In practice, to maintain ΔV_{OUT} or V_{OS} within the specifications, the output capacitance value will be higher to factor for the contribution of the capacitor devices parasitic resistance and inductance (ESL and ESR). However, this is not considered in this study, as the focus is on analyzing the initial design versus the number of phases.

3.2.4 *Two-Phase Coupled Inductor Analysis*

The basics of coupled inductor analysis are presented in [79], [86], where negative coupling has been shown to provide the best potential size reduction for buck converters. Using formulae for equivalent phase inductance, L_{SS}, presented in [79] for a 2-phase coupled buck converter operating with 180^{O} phase shift, normalized steady-state equivalent phase inductance L_{SS_norm} is expressed as:

$$L_{SS\_norm} = \frac{L_{SS}}{L_{Self}} = \begin{cases} \dfrac{1 - {k_f}^2}{1 + \dfrac{Dk_f}{1 - D}} & D \leq 0.5 \\ \dfrac{1 - {k_f}^2}{1 + \dfrac{(1 - D)k_f}{D}} & D > 0.5 \end{cases} \tag{3.15}$$

where k_f is the coupling factor, and L_{Self} is the non-coupled self-inductance of the inductor per phase, which is considered the baseline for normalization.

Steady-state phase inductance determines the peak-to-peak phase current ripple ΔI_{Ph}. L_{SS_norm} is plotted in Fig. 3.5(a) at different coupling factor values; it shows areas of L_{SS} enhancement (>100%) and roll-off (<100%). It also indicates coupling effect on the duty cycle range for equivalent ripple operation, i.e. where L_{SS_norm} = 100%. As seen in Fig. 3.5(a), L_{SS_norm} is impacted depending on the duty cycle range and the coupling factor. Hence, the coupling factor is analyzed for certain L_{SS_norm} values (3.15), which offers a better way of choosing the k_f value for a typical operating duty cycle range. From (3.15), the derived formula of k_f at $L_{SS\_norm} = x$ is expressed as:

$$K_f(x, D) = \begin{cases} \dfrac{xD + \sqrt{D^2(x^2 - 4x + 4) + 8D(x - 1) - 4x + 4}}{2(D - 1)} & D \leq 0.5 \\ \dfrac{xD - x - \sqrt{D^2(x^2 - 4x + 4) + 2xD - x^2}}{2D} & D > 0.5 \end{cases} \tag{3.16}$$

Another aspect of coupling is maximizing the steady-state phase inductance. That coupling factor is found by solving $\frac{d}{dk_f} L_{SS\_norm} = 0$, which represents maximum L_{SS_norm} trajectory, and it is expressed as:

$$K_{f\_Lmax} = \begin{cases} \dfrac{D - 1 + \sqrt{1 - 2D}}{D} & D \leq 0.5 \\ \dfrac{D - \sqrt{2D - 1}}{D - 1} & D > 0.5 \end{cases} \tag{3.17}$$

In Fig. 3.5(b), coupling factor is plotted at L_{SS_norm} = 100% and 90%, and maximum L_{SS_norm} trajectory. Fig. 3.5(b) addresses coupling factor selection guidelines for a wide duty cycle range. It shows the maximum coupling factor to maintain L_{SS_norm} at 100% and the coupling factor that maximizes the phase inductance if desired. Hence, to maintain $L_{SS\_norm} \geq$ certain value over the operating duty cycle range, the minimum $|k_f|$ value should be selected. For example, for $L_{SS\_norm} \geq$ 90% over duty cycle range (0.27~0.72), k_f should be ≤ -0.527, while for $L_{SS\_norm} \geq$ 100%, k_f should be ≤ -0.375. This selection guide

maintains an effective operation of the multiphase buck converter with a 2-phase coupled inductor by clarifying the range of operation over which the advantage of inductance enhancement is achieved. It is acknowledged that phase-shedding for light-load management can only occur for non-coupled phases or sets of coupled phases.

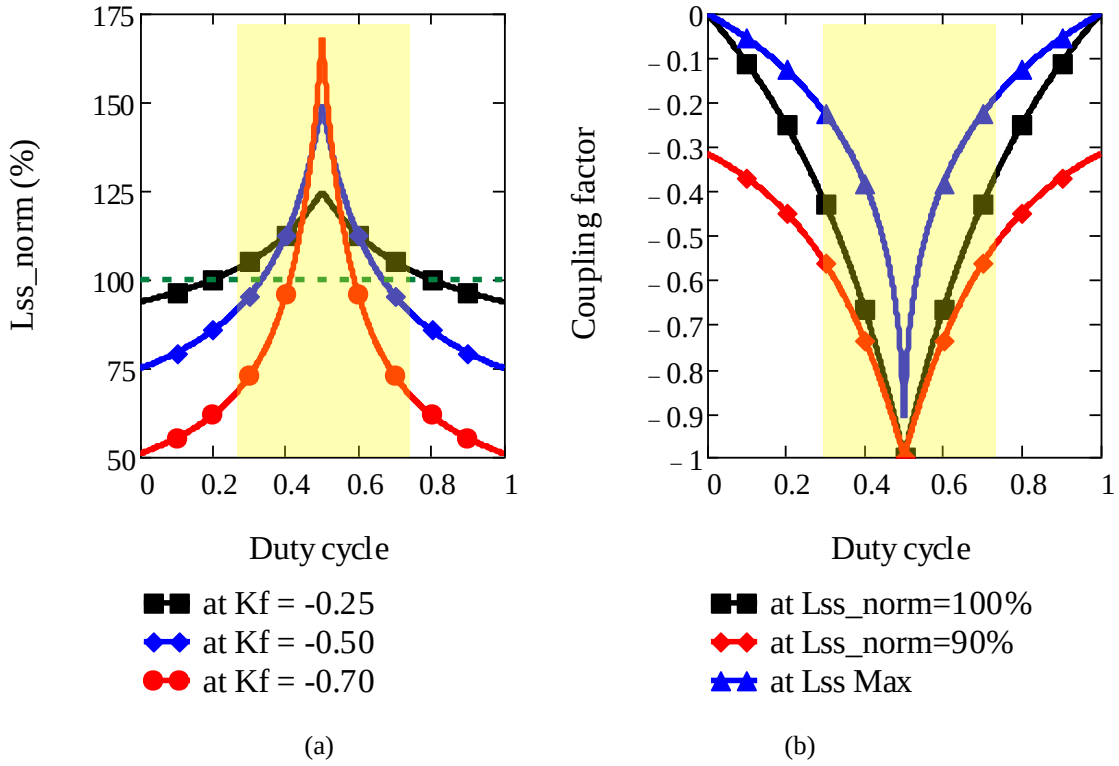


Fig. 3.5 2-phase coupled inductor analysis (a) L_{SS_norm} vs duty cycle at different k_f values, (b) k_f vs duty cycle at different L_{SS_norm} conditions.

3.2.5 *Theoretical Analysis Summary*

The presented theoretical analysis summarises that:

- Accounting for limited per-phase peak current in a multiphase buck converter results in a minimum achievable inductance and inductor peak energy.
- For the same phase ripple current limit, the minimum total inductor energy is the same for different numbers of phases.
- Increasing the number of phases in a very wide duty cycle converter can reduce the passives' peak energy. However, a small number of phases can optimise the passives for a relatively narrow duty cycle range.
- Minimum inductor peak energy is achieved for a current ripple level of 200%.

- Coupling factor in a wide duty cycle coupled inductor should not exceed a certain value to avoid degradation of steady state phase inductance, which can result in unexpected phase current increase.

3.3 *Demonstrator Converter design*

The considered converter specifications are listed in Table 3.1, which is a typical Point-of-Load (POL) step-down specifications for battery-powered applications. For this specification, the duty cycle ranges from 0.27 to 0.72, assuming ideal converter components; this is the same range as indicated by shading in Section 3.23.2 results. This study is a part of a project focused on integrated DC-DC converters with a 10-100 MHz switching frequency range, so the switching frequency is chosen at 20 MHz for easy prototype implementation on a PCB.

Table 3.1 Converter design specifications.

Symbol	Quantity	Value	Unit
F_{SW}	Switching frequency	20	MHz
V_{IN}	Input voltage	2.5 – 6.6	V
V_{OUT}	Output voltage	1.8	V
I_{DC}	Output DC current	3	A
ΔI_{Nph}	Output current ripple	0.75 (25%)	A
ΔV_{OUT}	Output voltage ripple	90 (5%)	mV
V_{OS}	V_{OUT} overshoot	90 (5%)	mV
I_{Low} to I_{High}	Load transient	0 to 3	A

The normalized analysis of Section 3.2 is useful to understand the theoretical impact of interleaving on passive components vs duty cycle while limiting the maximum limit of $\Delta I_{ph\%}$. However, the real converter design accounts for the maximum required values over the operating duty cycle range, which this section considers. The required inductance in a 1-phase buck converter is always higher at a lower duty cycle, but this does not necessarily apply to the multiphase converter as the maximum required inductance can be found somewhere in the middle of the duty cycle range. This is considered in the design procedure, i.e. summarised in the flowchart in Fig. 3.6. The design procedure in Fig. 3.6 starts by setting the converter specifications, then ΔI_{Ph} (3.1)-(3.4) is calculated over the range of duty cycle at each N_{Ph} value and maintained $\leq 2I_{Ph\_DC}$. Then other parameters are calculated, mainly L_{Ph}, which is required to calculate I_{Ph_PK}, E_{L_PK} and

C_{Out_Tr}. L_{Ph} and k_f are also calculated for the inductor design in the next section. Then ΔI_{Nph} value is updated to get its maximum value to estimate C_{Out_SS}.

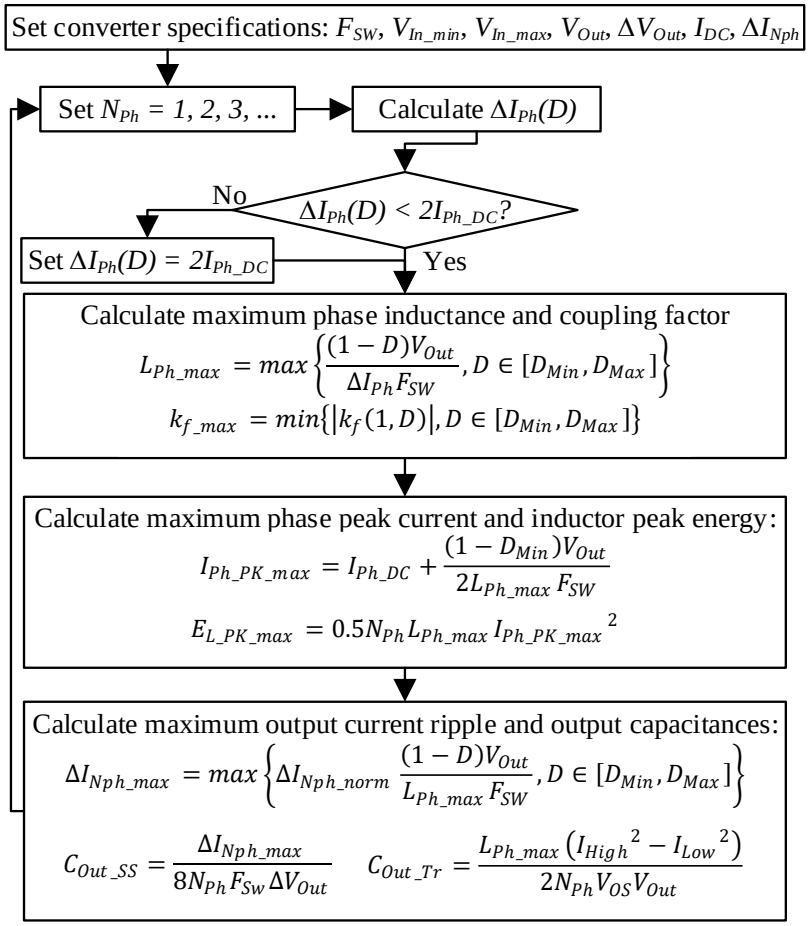


Fig. 3.6 Design procedure of multiphase buck converter.

Based on the previously explained design procedure, passives analysis is presented in Fig. 3.7 for converter specifications in Table 3.1 at $\Delta I_{ph} \leq 2I_{Ph\_DC}$ and unrestricted ΔI_{ph}. Results in Fig. 3.7(a) show that for $N_{ph} > 3$, total inductance continues to increase with increasing phase count due to limiting the maximum ΔI_{ph} to 200%. Inductor peak energy at $\Delta I_{ph} \leq 2I_{Ph\_DC}$ in Fig. 3.7(b) reduces to a minimum and remains constant for more than three phases. However, the percentage energy reduction relative to a 1-phase is more significant for 2-phase (at 48.4%) than 3-phase (at 39.5%). Results with unrestricted ΔI_{ph} in Fig. 3.7(a, b) show that while L_{Tot} does not increase with N_{Ph} increase, E_{L_PK} increases significantly.

The 2-phase option offers a better overall solution considering the additional space and circuit complexity required for extra phases of switches and control, which correlates with the normalized analysis predictions in Fig. 3.3(b).

Fig. 3.7(c, d) shows the normalized output capacitance for the steady-state ripple requirement, $C_{Out\_SS\_norm}$ and load transient requirement, $C_{Out\_Tr\_norm}$. As $C_{Out\_Tr\_norm}$ >> $C_{Out\_SS\_norm}$; the reduction in $C_{Out\_Tr\_norm}$ is more important. For 2-phase, $C_{Out\_Tr\_norm}$ is 0.74 µF (31.25%) and remains at 0.3 µF (12.5%) for 3-phase and higher, which correlates with the normalized analysis in Fig. 3.4(b). While a reduction in capacitance is welcomed, the capacitors' size is usually much smaller than inductors. Therefore the optimum phase count is usually determined by the inductor size.

In terms of two coupled inductors, a suitable coupling factor (k_f) can be determined with the aid of Fig. 3.5(b). For the converter duty cycle range from 0.27 to 0.72, the maximum k_f is -0.37 to prevent steady-state phase inductance rolling-off to below 100%. So, this restriction must be considered in the coupled inductors design. With a coupling factor of -0.37, the application of (3.15) shows that L_{SS_norm} varies between a minimum of 100% to a maximum of 137% based on the operating duty cycle.

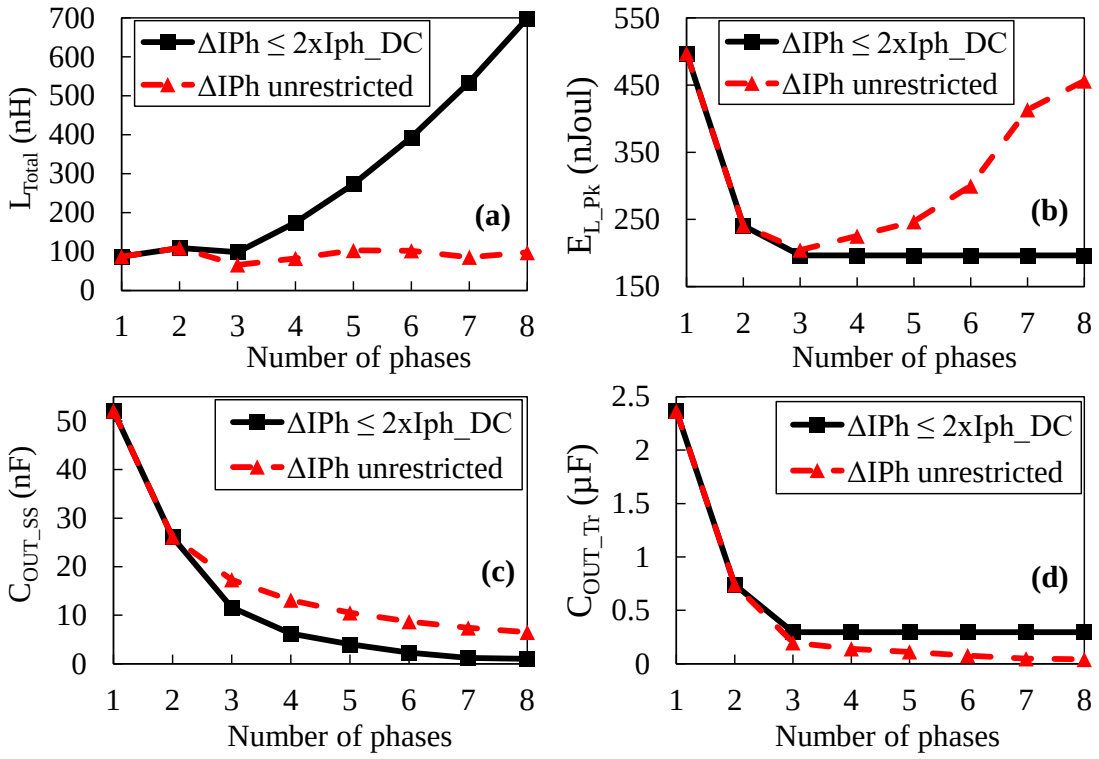


Fig. 3.7 Passives' analysis vs N_{Ph} for converter specification listed in Table 3.1 at ΔI_{Ph} < 2x and 100x $2I_{Ph\_DC}$,100x limit is considered the unrestricted ΔI_{Ph} case: (a) L_{Tot}, (b) E_{L_PK}, (c) C_{Out_SS}, (d) C_{Out_Tr}.

3.4 *PCB Inductor Design*

Fig. 3.7 explains the impact of increasing the number of phases in terms of passives. However, these relative results may differ from the actual inductor size when manufacturing capabilities and limitations are included, which is discussed in this

section. For the prototype design, spiral and solenoid air-core inductors on FR4 double layer PCB are considered. The PCB manufacturing capabilities include copper thickness of 35 µm, minimum trace and gap width of 0.15 mm, minimum via diameter of 0.2 mm, and PCB height of 1.6 mm. To minimize inductor size, the conductor width for the inductor is calculated according to the standard IPC-2221A [87] for a temperature rise of 50 ^{O}C. However, future work can use the newer standard IPC-2152 [88], [89]. Conductor trace width may also be chosen to meet specific resistance requirements according to the allowable overall inductor power loss.

These assumptions determine the conductor width for a phase inductor, i.e. 0.52 mm in 1-phase and 0.21 mm in 2-phase. However, for solenoid inductors, the minimum via-to-via distance (including the surrounding annular ring and solder mask) results in extra space utilized to increase the minimum conductor width to 0.37 mm, which improves the inductor DC resistance. This shows how PCB design rules impose a limiting factor on PCB inductor size reduction.

3.4.1 *PCB Spiral Inductor Design*

The spiral inductor inductance is calculated as in [90]:

$$L_S = 0.5\mu_0 N_{Layers} {N_T}^2 Dia_{Avg}\left(ln\left(\frac{2.46}{P}\right) + 0.2P^2\right) \tag{3.18}$$

where μ_0 is the air permeability $\mu_0 = 4\pi 10^{-7}$, N_T is the number of turns, N_{Layers} is the number of the PCB series-connected layers, Dia_{AVG} is the average spiral diameter $Dia_{Avg} = 0.5(Dia_{Out} + Dia_{In})$, and P is the spiral fill factor:

$$P = \frac{Dia_{Out} - Dia_{In}}{Dia_{Out} + Dia_{In}} = \frac{1 - Dia_{Ratio}}{1 + Dia_{Ratio}} \tag{3.19}$$

where $Dia_{Ratio} = Dia_{In} / Dia_{Out,}$ which is the inner to outer diameter ratio. Then the spiral inductor inductance is analyzed as a function of Dia_{Ratio}.

DC resistance of the spiral inductor is calculated as:

$$R_{DC} = \frac{\rho N_{Layers} \ell_{Spiral}}{W_C T_C} \tag{3.20}$$

where ρ is the copper conductivity 1.72x10^{-8} Ωm, ℓ_{Spiral} is the spiral inductor length per layer, W_C and T_C are the conductor width and thickness, respectively, for a rectangular cross-section conductor. ℓ_{Spiral} is derived and expressed as:

$$\ell_{Spiral} = \int_0^{2\pi N_T} \sqrt{\left(R_{In} + \frac{W_C}{2} + \frac{W_C + S_C}{2\pi}\theta\right)^2 + \left(\frac{W_C + S_C}{2\pi}\right)^2}\, d\theta \tag{3.21}$$

where R_{In} is the inner radius, S_C is the conductor spacing.

Then the inductor DC quality factors is calculated:

$$Q_{DC} = \frac{2\pi F_{SW} L_S}{R_{DC}} \tag{3.22}$$

With the aid of the previous formulas, the spiral inductor is analyzed versus Dia_{Ratio}. Fig. 3.8(a) shows the analysis for a 1-phase double-layer 90 nH spiral inductor in terms of Q_{DC} and footprint area as a design example for the 1-phase converter in Table 3.2. Dia_{Ratio} was chosen at 0.3155 for this 1-phase 90 nH inductor as a balanced point where Q_{DC} (156) is slightly close to the peak value (158), and the inductor area (35.1 mm^2) is close to the minimum value (32.7 mm^2), this balance is reflected on $Q_{DC}/Area$ value.

3.4.2 *PCB Solenoid Inductor Design*

Based on the solenoid inductance basic equation, the PCB solenoid inductance is calculated approximately as:

$$L_S = \frac{\mu_0 {N_T}^2 (W_{Sol} - 2D_{Via})(H_{Sol} - 2T_C)}{(N_T + 1)W_C + N_T S_C} \tag{3.23}$$

where D_{Via} is the PCB via diameter, and W_{Sol} and H_{Sol} are the inductor's overall width and height.

DC resistance of the solenoid inductor is calculated as:

$$R_{DC} = (N_T + 1)R_{DC\_st} + N_T\left(R_{DC\_dia} + 2R_{DC\_via}\right) \tag{3.24}$$

where R_{DC_st}, R_{DC_dia} and R_{DC_via} are DC resistances of straight conductors, diagonal conductors, and PCB via, respectively.

Inductor design analysis regarding footprint area and Q_{DC} is presented in Fig. 3.8(b) vs. the number of turns for a 1-phase 90 nH solenoid. As seen in Fig. 3.8(b), at a small number of turns, Q_{DC} is small, and the inductor area is large, so, for this design, the turns count should not be less than 5. For the prototype 1-phase 90 nH inductor design of Table 3.2, 6 turns design is suitable. At N_T = 6, W_C = 0.52 mm and S_C = 0.15 mm, a 90 nH solenoid has Q_{DC} = 126 and area = 28.6 mm^2 approximately.

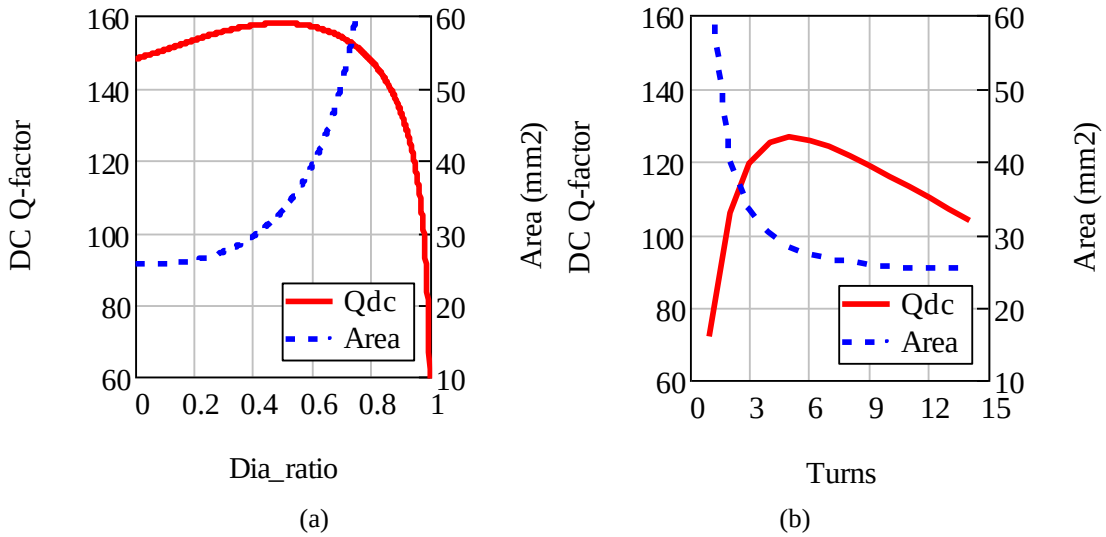


Fig. 3.8 Q_{DC} and inductor area for 1-phase 90 nH double layer inductor designs with W_C = 0.52 mm and S_C = 0.15 mm: (a) Spiral, (b) Solenoid.

3.4.3 *PCB Inductor Implementation*

Using the procedure described in section 3.4.2 a range of solenoid inductors were designed for N_{Ph} = 1~5 as presented in Fig. 3.9. While results of E_{L_Pk} in Fig. 3.7 suggest that a reduction in inductor size should be achieved, due to the PCB manufacturing limitations, inductor size increases for $N_{Ph} > 3$, and further loss reduction is insignificant. Besides, the maximum inductance density was achieved at 2-phase with no benefit achieved by adding more phases. Therefore, $N_{Ph} \geq 3$ inductors were discarded from implementation and testing.

Details of the selected inductor designs and Finite Element Analysis (FEA) simulation results are compared in Table 3.2. FEA simulation was done at a low frequency (1 Hz) to verify L_S, R_{DC} and coupling factor values. These results show good agreement (<10%) with the calculation models presented in Section 3.4. However, a more accurate analytical model may be required for higher frequencies, as in [91]. Single and two-phase versions of spiral and solenoid inductors were designed for comparison as described in Section 3.2. One coupled spiral design was considered.

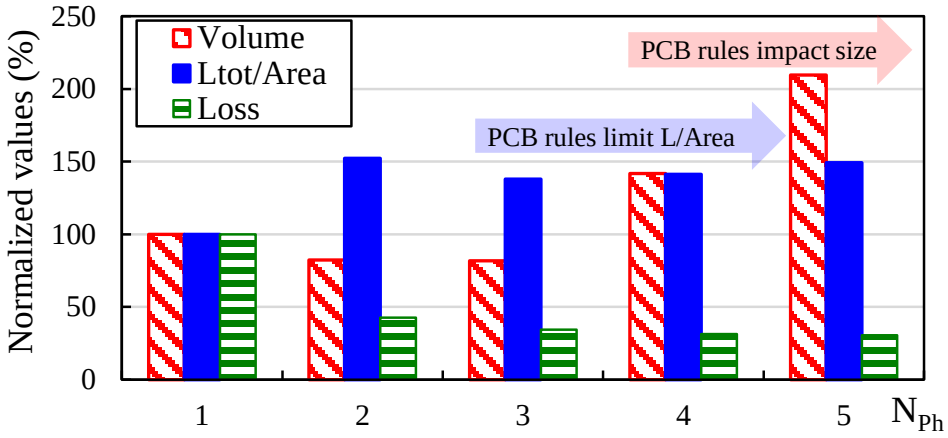


Fig. 3.9 Multiphase solenoid inductor design in terms of peak energy, volume and loss normalized to 1-phase inductor.

Inductor DC and AC losses were extracted from spice simulation at V_{IN} = 2.5 & 6.6 V based on measured R_{DC} and R_{AC} and are presented in Table 3.2. It shows that 2-phase compared to 1-phase inductors generally have lower DC loss. For 2-phase inductors, AC loss is significantly higher at V_{IN} = 6.6 V due to higher ripple current, so this predicts a lower light load efficiency at higher V_{IN} values. Accordingly, inductor efficiency vs output power is presented in Fig. 3.10.

$$Ind\ efficiency = \frac{P_{Out}}{P_{Out} + P_{Ind\_Loss}} \tag{3.25}$$

For 1-phase converter designs, the spiral inductor full load efficiency is only 1.53% & 1.47% higher than the solenoid inductor at V_{IN} of 2.5 & 6.6, respectively; however, its area is 21% bigger than the solenoid one. This means a 1-phase solenoid inductor utilises area better than a 1-phase spiral inductor on a double layer PCB considering the same manufacturing constraints.

Comparing the 2-phase spiral and solenoid designs shows that the solenoid design is more efficient for approximately the same inductor footprint area. Fig. 3.10 indicates that the 2-phase solenoid inductors (2Ph_Sol) have the best overall efficiency over the output power range starting from 0.36 W at 2.5 V_{IN} and from 1.8 W at 6.6 V_{IN}. It achieved a maximum inductor efficiency of 97.2% and 92.8%, and full load inductor efficiency of 92.2% and 90.9% at V_{IN} of 2.5 V and 6.6 V, respectively.

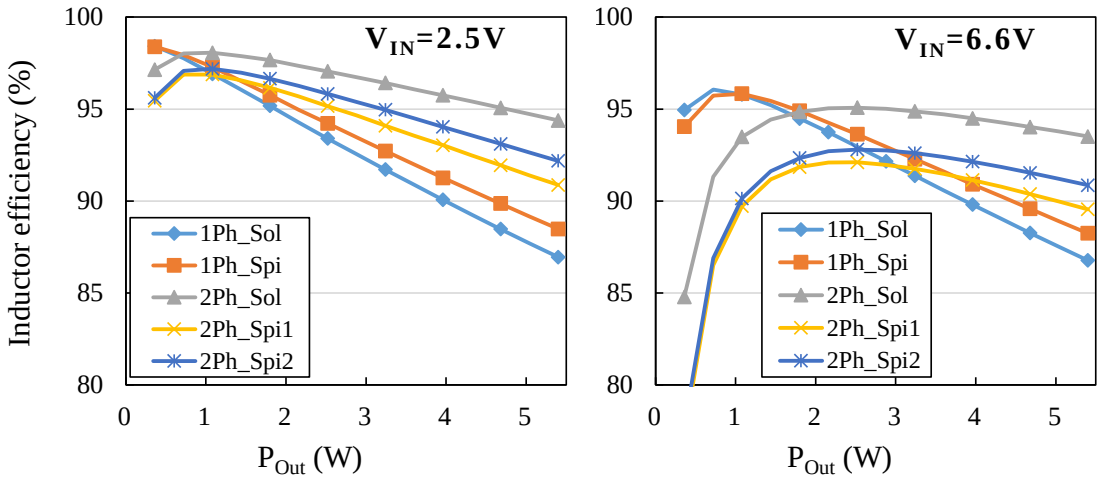
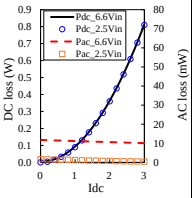
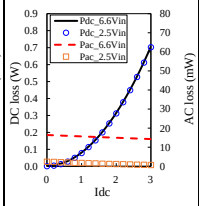
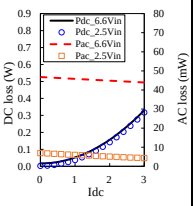
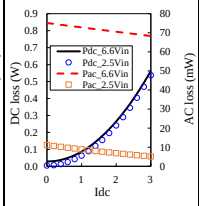
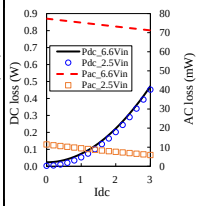
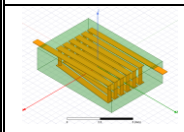
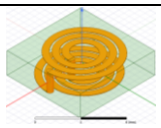
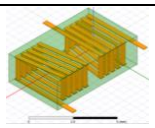
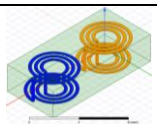
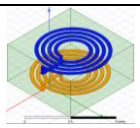
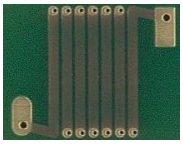
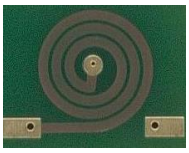
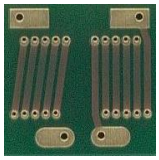
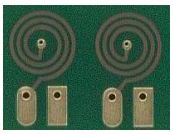
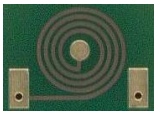


Fig. 3.10 Calculated inductor efficiency based on measured R_{DC} and R_{AC}.

Concerning coupling, it was found that the 2-phase coupled spiral inductor 2Ph_Spi2 (with k_f = 0.2) achieved 1.3% higher inductor efficiency at full load, with 22.7% smaller area (i.e. 19.8 mm^2) when compared to the non-coupled spiral (2Ph_Spi1). The 2Ph_Spi2 configuration has an opposing spiral on each layer, which results in partial field cancellation and better Electromagnetic Interference (EMI) performance than 1-phase spiral, which is known for noise radiation [92]. However, detailed EMI performance is not in the scope of this study. The coupling factor of 0.2 was set by the inductor geometry, determined by the PCB manufacturing capabilities. While this is lower than the recommended value of 0.37, it still results in up to 20% increase in steady-state inductance, resulting in up to 20% reduction in peak-to-peak phase current ripple, and therefore AC losses.

Table 3.2 Selected inductors' designs.

Design		1Ph_Sol	1Ph_Spi	2Ph_Sol	2Ph_Spi1	2Ph_Spi2
No of phases		1	1	2	2	2
Inductor type		Solenoid	Spiral	Solenoid Axial	Spiral Side by side	Spiral Axial (coupled)
L_{Ph} (nH)		90	90	54.3	54.3	54.3
I_{Ph_DC} (A)		3	3	1.5	1.5	1.5
Calc	R_{DC} (mΩ)	90	72.6	57	106	93
	Area* (mm^2)	28.6	35.1	26	25.6	19.8
	Q_{DC}	126	156	122	64	73
FEA 1Hz	L_S (nH)	92.7	96.9	55.5	56.9	57.1
	R_S (mΩ)	82	71	63	108	96
	k_f	-	-	-0.024	-0.015	-0.2

Design	1Ph_Sol	1Ph_Spi	2Ph_Sol	2Ph_Spi1	2Ph_Spi2
Q at F_{SW}	143	170	110	66	75
Measured R_{DC}, R_{AC} at F_{SW} (mΩ)	90, 266.7	78, 372.1	70, 193.2	119, 310.3	100, 319.5
Inductor loss based on measured R_{DC} and R_{AC} at V_{IN} = 2.5 & 6.6 V					
FEA model					
Manufactured PCB inductors					

3.5 *Converter Modelling and Measurements*

In this section, the converter's performance with the designed and manufactured 1 & 2-phase solenoid and spiral inductors presented in Section 3.4. Converters are based on EPC2040 GaN FET switches [93] used for each phase's high and low sides. The EPC2040 is rated for 15 V and 3.4 A, and it has a total gate charge of 745 pC, which makes it a good candidate for 20 MHz switching frequency.

3.5.1 *Calculated loss breakdown*

Fig. 3.11 shows a comparison of the inductors area and the calculated converter loss breakdown at full load of 5.4 W and nominal V_{IN} of 4.5 V. The converter losses calculations are based on data for EPC2040 switches [93] and formulas guidelines in [94], and inductor loss is calculated as in Table 3.2. In Fig. 3.11, the 1-phase converters' FETs have higher conduction loss and lower switching loss than 2-phase converters due to using the same switches for all cases. It may be an unfair comparison, but this is because EPC2040 is the lowest rated and smallest GaN FET so far in the market making it the most suitable FET for 20 MHz operation.

In Fig. 3.11, 2Ph_Sol achieves the smallest overall loss (0.82 W), mainly due to inductor conduction loss reduction while having nearly the same overall area as other 2-phase inductors. The coupled configuration 2Ph_Spi2 design achieves a smaller overall loss

(85.3 mW less) with a smaller inductor area (5.8 mm^2 less) against the non-coupled 2Ph_Spi1.

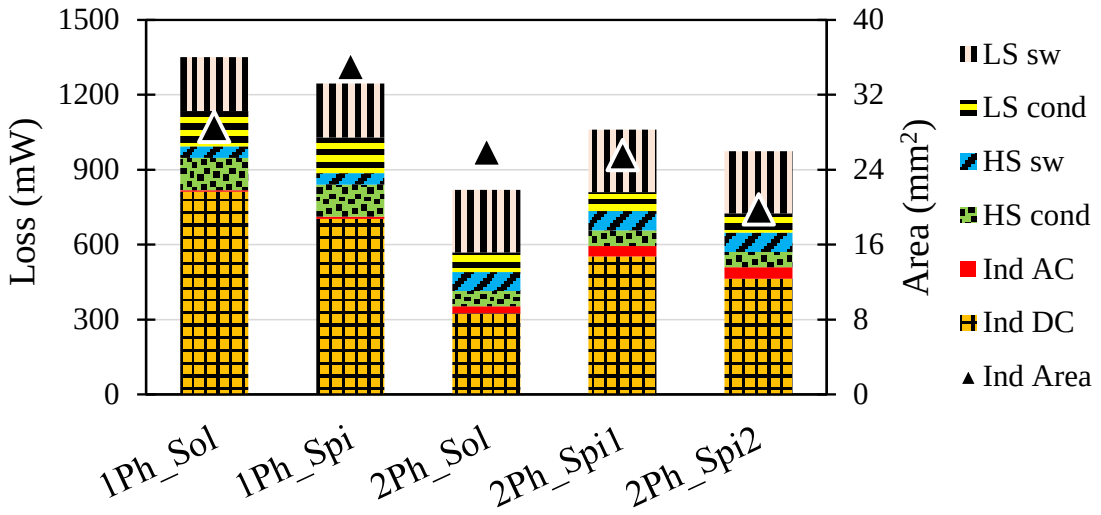


Fig. 3.11 Calculated full load loss breakdown at V_{IN} = 4.5 V and inductor area.

3.5.2 *Simulation and measurements*

Fig. 3.12 and Fig. 3.13 present the prototype converter schematic and picture indicating the components, and test bench setup is shown in Fig. 3.14. The EPC2040 switches are driven by a Peregrine PE29102 gate driver, capable of 40 MHz [95]. The PWM input signal is generated using a DIGILENT Nexys3 FPGA development board, i.e. Xilinx Spartan-6 LX16 FPGA chip. The FPGA was programmed to generate a 20 MHz signal with the duty cycle adjusted externally. The deadtimes during rising and falling are adjusted manually using external variable resistors, as shown in Fig. 3.12, to minimize the over/undershoot in the switching voltage V_{SW} signal. The load is an electronic resistive load, so the output current is reflected in the V_{Out} signal.

Measured waveforms for 1&2 phase operation are shown in Fig. 3.15. Although the PCB parasitic effects on the FPGA signal (V_{PWM}) in Fig. 3.15(a), it does not affect the gate driver operation as seen in V_{GS_LS} signal. Fig. 3.15(a, b) also shows reasonable V_{SW} over/undershoot values. Induced interference voltages were created in the ground loop of the voltage probes. However, for efficiency measurements, no voltage probes were attached to reduce the effect of the oscilloscope added capacitances and ground loops to the circuit. Efficiency was measured in terms of DC voltage and current at the converter input and output.

Simulation and measured converter efficiencies are shown in Fig. 3.16(a)&(b) respectively at the nominal V_{IN} = 4.5 V, V_{OUT} = 1.8 V and F_{SW} = 20 MHz. Converter simulation was performed with LTspice software, including EPC2040 spice models. Deadtimes between high and low side gate driver signals were tuned in the simulation to reduce overall switching loss. Measured efficiency was adjusted to account for the DC losses in the inductor interconnecting wires (20 mΩ per phase approximately).

Fig. 3.16 shows a good match between simulation and measured converter efficiency at light loads and the trend in relative efficiency for different inductors; however, there is a mismatch that increases with the load increase. There are possible reasons for this, e.g. the impact of the high switching frequency or temperature on the GaN FETs dynamic resistance, as described in [96] and [97] (but not yet characterized for EPC2040), the common source inductance in the gate driver loop [94], deadtime adjustment, or PCB parasitic effects, which will be investigated further in future work. Nonetheless, the 2-phase converter with the non-coupled solenoid inductors (2Ph_Sol) has a better efficiency curve than other configurations, correlating with the results trend in Fig. 3.10, while there is a slight improvement provided by coupled vs. non-coupled 2-phase spiral inductors.

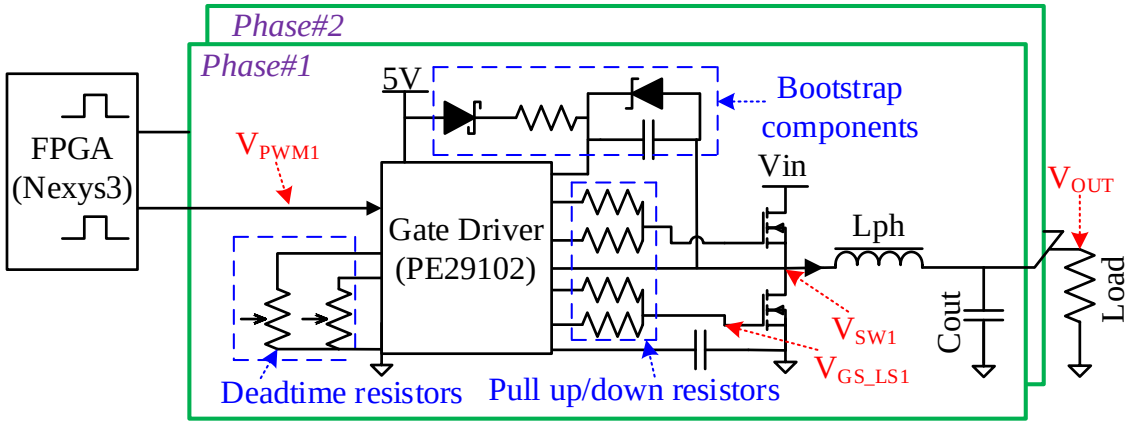


Fig. 3.12 Circuit schematic of the prototype converter.

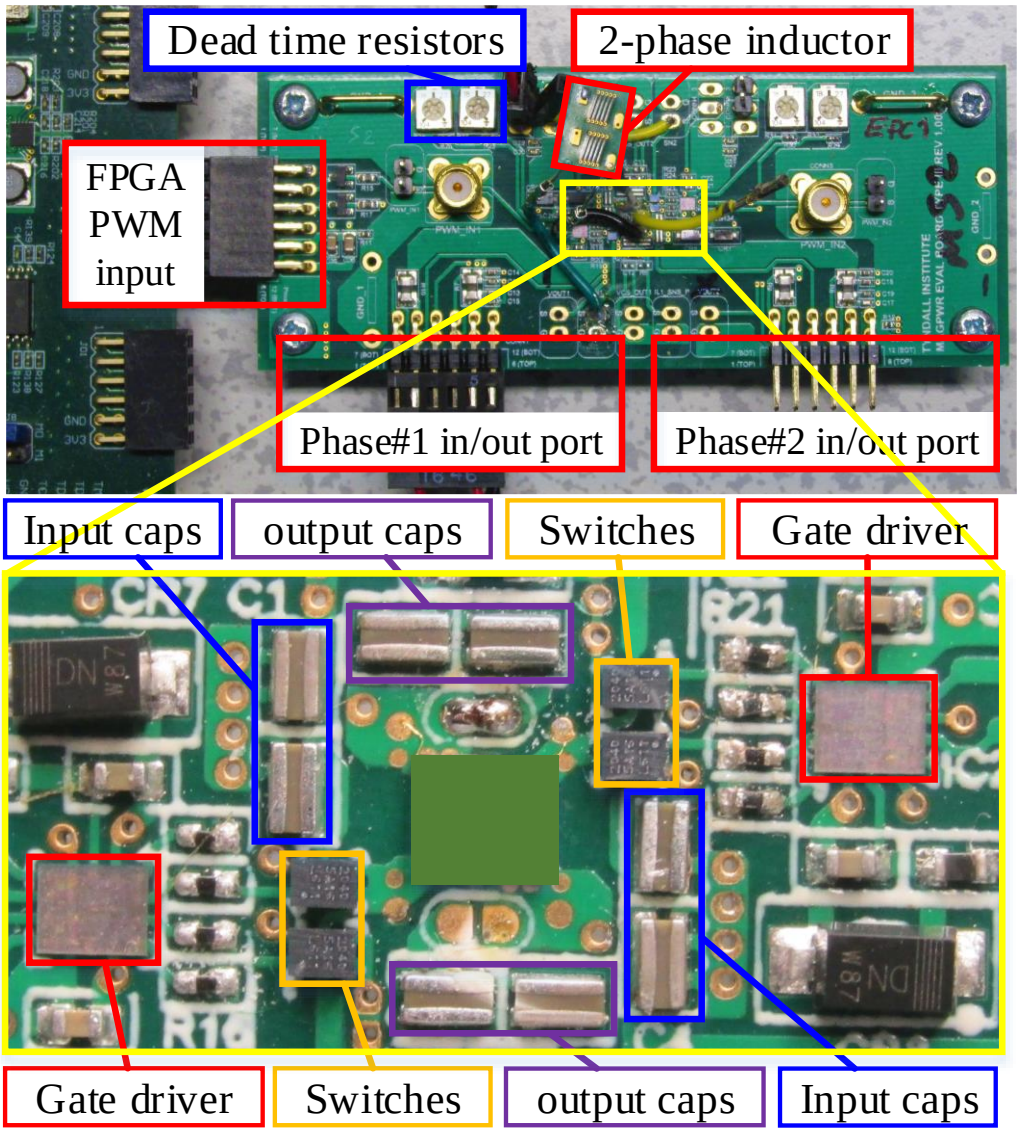


Fig. 3.13 Picture of the prototype converter.

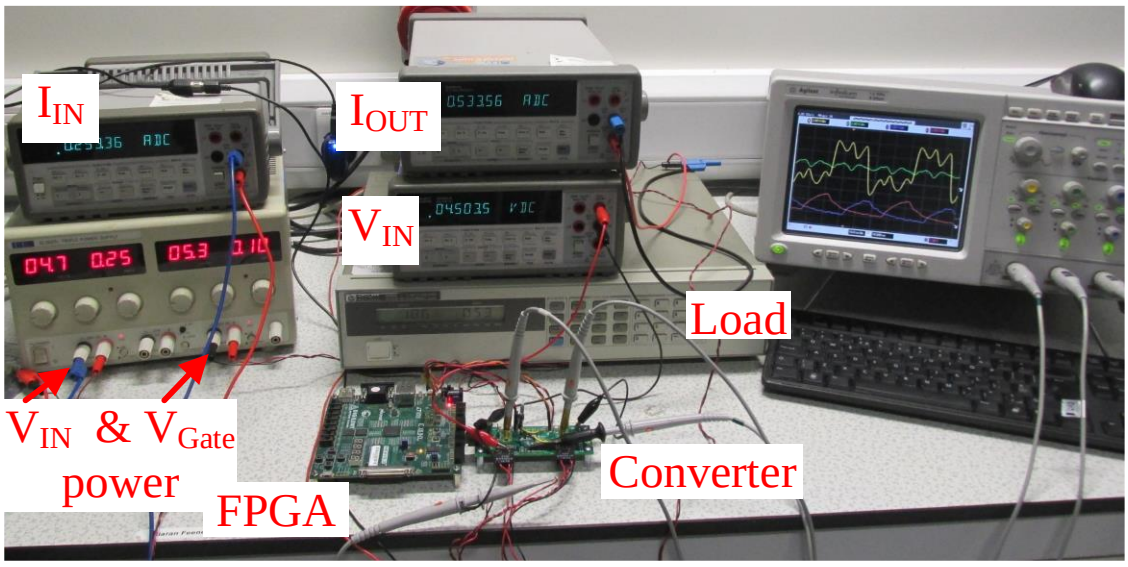
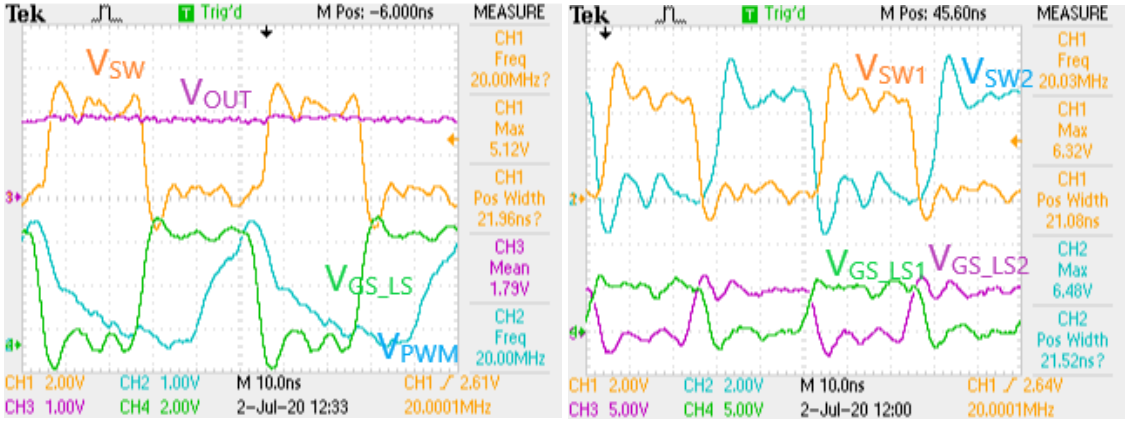


Fig. 3.14 Picture of the test bench setup.



(a) (b)

Fig. 3.15 Testing waveforms at 20 MHz, V_{IN} = 4.5 V, V_{OUT} = 1.8 V: (a) 1-phase V_{PWM}, low side FET V_{GS}, V_{SW}, V_{OUT}, (b) 2-phase low side FETs V_{GS}, V_{SW}.

Table 3.3 shows that the implemented inductors achieved high inductance density compared with other converters that employed air-core inductors in buck topology. This results from the proposed design procedure to optimize the number of phases selection and the inductor design procedure to choose the optimum design point to maximize Q_{DC} while minimizing the inductor area.

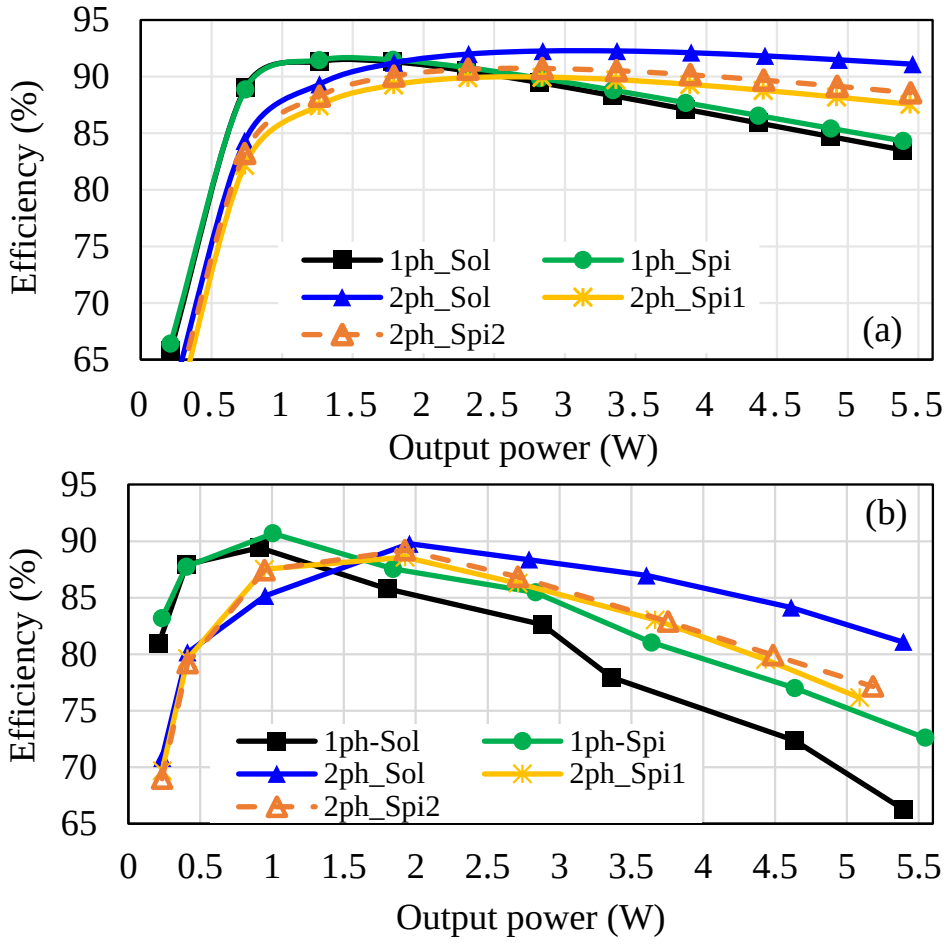


Fig. 3.16 Converter efficiency at V_{IN} = 4.5 V (a) Simulation, (b) Measured.

Table 3.3 Comparison with converters that employed air-core inductors in buck topology.

Reference	[98] **Single turn**	[40] **Spiral**	[5] **Spiral**	[17] **Solenoid**	**This work**	
					2Ph_Sol	**2Ph_Spi2**
Inductor technology	Co-packaged	PCB 4 layers	On-chip 65nm	Co-packaged	PCB 2 layers	
N_{Ph}	1	1	2	4	2	
V_{IN} (V)	1.7	12	2-2.2	1.6	2.5-6.6	
V_{OUT} (V)	1	1.8	0.7-1.2	1.1	1.8	
I_{DC} (A)	0.8	5.5	0.7	4.4	3	
F_{SW} (MHz)	200	1-5	500	150	20	
$L_{Total}/Area$ (nH/mm^2)	0.68	1.45	8.6	1.97, 0.93	4.18	5.48
η_{Max} (%)	93	78.5	76.2	89.5	89.8	89.2

3.6 *Summary*

A detailed normalized analysis of passives in multiphase interleaved buck converter is presented in terms of total inductance and output capacitance for steady-state and load transient requirements considering wide input voltage converter specifications and phase current ripple limitations. The analysis shows that for a wide input voltage converter specification and restricted phase current ripple, the passive components' peak energy will saturate to a minimum limit at a certain number of phases. Hence, increasing the number of phases is not necessarily going to reduce the size of the passive components. The peak energy will increase after this saturation point in the case of unrestricted phase current ripple.

This chapter builds on the previous literature coupled inductor analysis to present a coupling selection guideline to either maintain or maximize the phase inductance over non-coupled inductors, applicable for wide input voltage specifications.

A straightforward procedure is proposed to analyze the passives in a multiphase buck converter for wide input voltage, which helps determine the optimum number of phases for various applications without the need for computational demanding optimization technique.

For validation, air-core PCB inductors were considered for ease of implementation and avoiding core loss non-linearity. The inductors were designed considering consistent

PCB manufacturing capabilities and a target temperature rise. The study shows that considering different inductor geometry affects the inductor efficiency and footprint area results. For both solenoid and spiral, the implemented 20 MHz converter confirms the predicted trends of 2-phase inductors being competitive to equivalent 1-phase inductors in terms of efficiency and size, even with practical considerations of wide-input voltage range and PCB design rules.

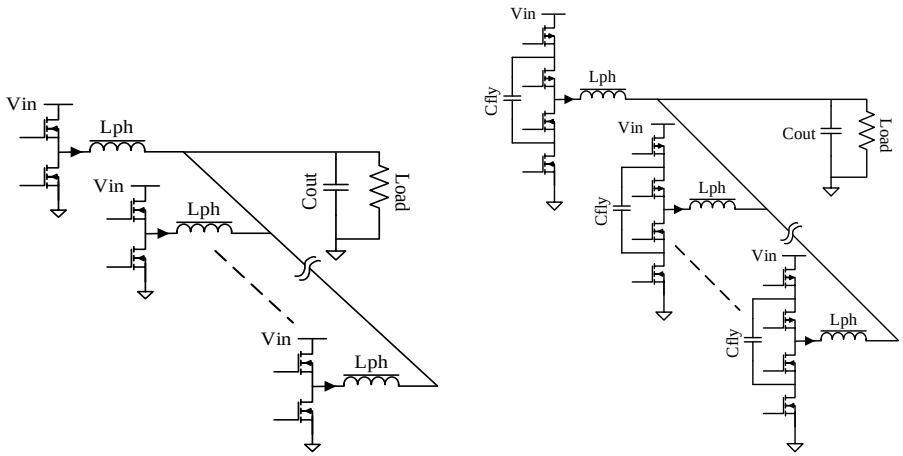
The combination of the optimum choice of the number of phases and the PCB inductor design resulted in high inductance density and high peak efficiency of the prototype compared with other literature. A similar analysis can be applied to inductors manufactured using other fabrication technologies as well.

Chapter 4 – Multiphase 3-Level Topology

In chapter 3, passive components in the multiphase buck topology (shown in Fig. 4.1(a)) are analysed to study the effectiveness of increasing the converter number of phases on the size and performance of the passive components. A similar study can be done on the 3-level topology (shown in Fig. 4.1(b)), as it is suitable for multiphase scaling. This chapter presents a comparative study between the multiphase buck and the multiphase 3-level topologies in terms of passive components considering practical specifications like wide input voltage range and limiting the maximum current ripple per phase. The study also compares 2-phase coupled inductor performance in both topologies.

4.1 *Introduction*

The 3-level converter is an inductor-based Flying Capacitor Multilevel (FCML) topology (also known as Hybrid-Switched Capacitor) and is a widely researched topic. An important advantage of FCML topology is the ability for a high step-down conversion ratio with reduced voltage stress on the switches [99]. In other words, it can utilise low voltage rated switches to step down higher input voltage. The FCML topology also results in a multiplied switching-node frequency with a reduced amplitude, which enables reduced output filter passive components [100], [101], because of the reduced inductor volt-seconds requirement and the increased ripple frequency. However, it requires a flying capacitor and extra gate drivers for each switching level, limiting the benefits of adding more switching levels.



(a) (b)

Fig. 4.1 Converter topology schematic: (a) multiphase buck, (b) multiphase 3-level.

Different SC-based topologies have been studied in multiphase interleaved configurations, as in [6], [12], [28], [102], [103]. However, to the best of the authors' knowledge, the impact of the number of phases in the multiphase 3-level converter on the passive components' size has not been addressed. Moreover, previous studies have investigated the coupled inductor in the multiphase buck topology [41], [60], [62], [79], [81], [82], [84]. However, no theoretical analysis has been published for a 2-phase negatively coupled inductor in a multiphase 3-level converter. This would be for selecting a suitable coupling factor for given converter specifications. This chapter addresses the impact of the number of phases on the passive components in a multiphase 3-level topology and corresponding 2-phase coupled inductor performance.

In relation to SC topologies themselves, there are different configurations, like FCML, Series-Parallel, and Dickson, as presented in [99][100]. Hybrid SC topologies are also an interesting research area, e.g. SC plus buck converter in [20], multioutput SC plus buck converter in [25], and a 2-phase converter with auto phase current balancing in [102]. SC can also be used in series with other topologies for multistage conversion, as in [26]. SC topology is also considered in different resonance converter configurations like Switched Tank Converter (STC) in [104][105], cascaded resonant converter in [103], and resonant SC for low power in [106][107].

4.2 *Multiphase Interleaved Buck Analysis*

As described in Chapter 3, the multiphase interleaved buck converter (shown in Fig. 4.1(a)) operates with interleaved phases with a phase shift of $360/N_{Ph}$ where N_{Ph} is the number of phases, so the overall sum of all phases is 360 degrees [84]. This interleaving causes the overall current ripple of the combined phases to cancel partially, resulting in a smaller amplitude output ripple with frequency multiplied. These characteristics may help to reduce the size of the required passives or improve converter performance.

The analysis aim in this chapter is similar to chapter 3. However, instead of developing normalised formulas, results are normalised relative to a single-phase buck converter after calculating the actual physical quantities, because the existence of a flying capacitor makes it difficult to normalise the multiphase 3-level topology to the single-phase buck topology in terms of theoretical passive component values, in addition to changes of the output capacitance calculation for load transient, which will be discussed in the coming sections.

4.2.1 *Inductance selection*

Inductance and inductor peak energy analysis were presented and discussed in chapter 3 for the multiphase buck topology. For ease of comparison with the 3-level converters in this chapter, total inductance normalised to a single-phase buck is shown in Fig. 4.2(a). It shows total inductance limited to a minimum value for a range of duty cycle varying with the number of phases due to limiting the maximum phase current ripple at 200%. Normalised inductor peak energy is presented in Fig. 4.2(d), and it shows a minimum limit value caused by limiting the phase current ripple. This means that increasing the number of phases is not necessarily going to help to reduce the inductors' size, as concluded previously in chapter 3.

4.2.2 *Output capacitance selection*

For steady-state operation, the output capacitance $C_{OUT\_B\_SS}$ can be calculated for the desired output voltage ripple ΔV_{OUT} after correcting the value of ΔI_{Nph_B} due to the applied limit on current ripple per phase ΔI_{Ph}. This correction was neglected in the normalised formulas in chapter 3.

$$C_{OUT\_B\_SS} = \frac{\Delta I_{Nph\_B}}{8 N_{Ph} F_{Sw} \Delta V_{OUT}} \tag{4.1}$$

where F_{SW} is the switching frequency.

However, output capacitance is practically calculated to limit V_{OUT} overshoot V_{OS} and undershoot V_{US} within tolerance during load transients [85]. Load transient output capacitance $C_{OUT\_B\_Tr}$ is calculated in (4.2) as in [108] for loading and unloading transient conditions assuming a fixed frequency PWM controller. Differently from chapter 3, output capacitance calculation accounts for the unloading state with the controller off time delay, which may result in $V_{US} > V_{OS}$. With this assumption, the output capacitance for load transient requirements $C_{OUT\_B\_Tr}$ is calculated as follows:

$$C_{OUT\_B\_Tr} = \begin{cases} \dfrac{N_{Ph} L_{Ph\_B} {I_{Ph\_dc}}^2}{2 V_{OS} V_{OUT}} & loading \\ \dfrac{I_{Ph\_dc}(1-D)}{V_{OS} F_{SW}} + \dfrac{N_{Ph} L_{Ph\_B} {I_{Ph\_dc}}^2}{2 V_{OS}(V_{IN} - V_{OUT})} & unloading \end{cases} \tag{4.2}$$

where V_{OUT} and V_{IN} are the output and input voltages, respectively.

$C_{OUT\_B\_SS}$ and $C_{OUT\_B\_Tr}$ are presented in Fig. 4.2(b, c), respectively, normalised to a single-phase buck value. It shows that limiting ΔI_{Ph} maximum value limits $C_{OUT\_B\_SS}$ at a maximum limit that varies with the number of phases; however, it limits $C_{OUT\_B\_Tr}$ at a minimum value for all numbers of phases. For output capacitor size representation, peak energy is calculated as $Epk_{Cout\_B} = 0.5\, C_{Out\_B}(V_{Out} + 0.5\, \Delta V_{Out})^2$, which is shown in Fig. 4.2(e, f) normalised to single-phase buck values.

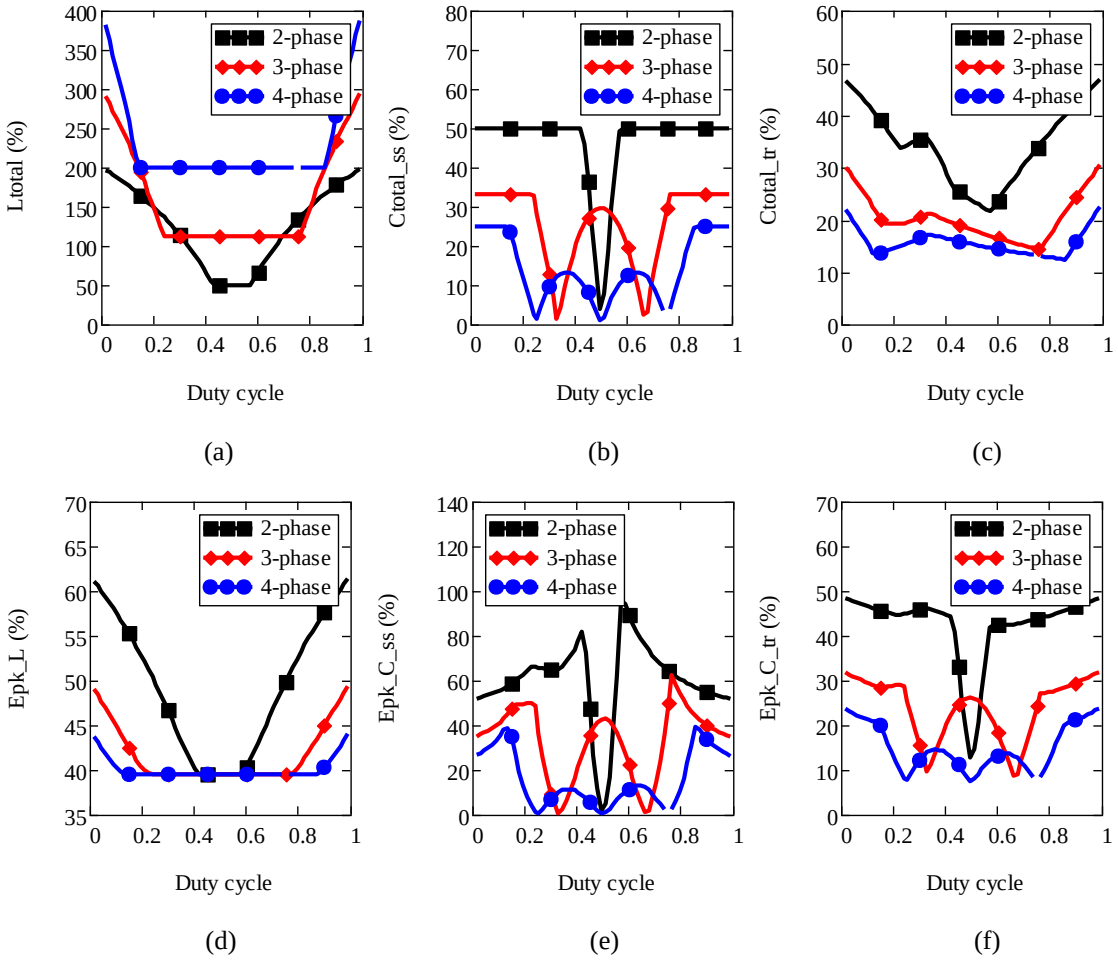


Fig. 4.2 Multiphase buck passives analysis normalised to single-phase buck.

4.3 *Multiphase 3-Level analysis*

The multiphase 3-level converter (shown in Fig. 4.1(b)) operates with interleaved phases similar to the multiphase buck, as explained in the previous section. The 3-level converter operation has been described in previous papers, such as [109][110]. Its main advantages are doubling the output voltage switching frequency while also halving its amplitude. This reduces the output filter components' size and the voltage stress on the switches. On the other hand, it requires four switches and associated gate drivers per phase, which can

be a limiting factor, particularly for light-load efficiency, solution size and control complexity.

4.3.1 *Inductance selection*

The overall output ripple reduction concept is applied as explained in chapter 3 for the multiphase buck, with the buck converter duty cycle replaced with the 3-level switching duty cycle. In the buck topology, the switching duty cycle (D) is ideally the voltage conversion ratio:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{T_{On\_sw}}{T} \tag{4.3}$$

where T is the switching period ($T=1/F_{SW}$), and T_{On_SW} is the switch turn on duration.

The 3-level converter operates in two modes, as explained in [109]. This can be extended to define the term of inductor duty cycle (D_{Ind_3L}) which can facilitate the calculation of the total output current ripple in the multiphase 3-level converter.

Fig. 4.3 shows the simulation gate-source voltages, switching node voltage and inductor current waveforms at different duty cycle values.

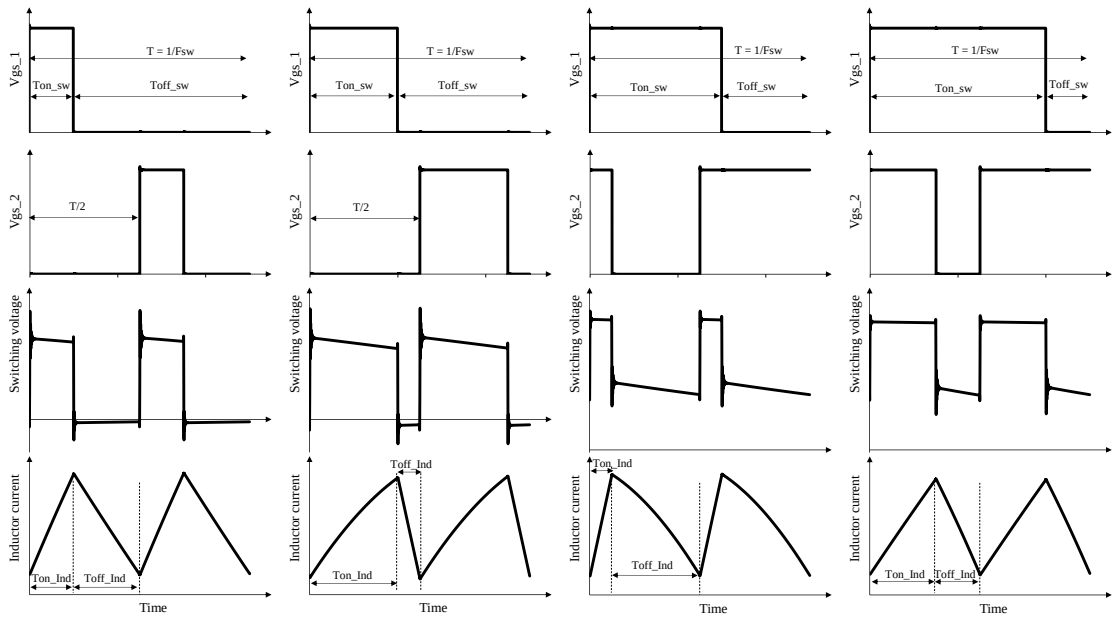


Fig. 4.3 3-level converter single switching cycle simulation waveforms at D= a) 0.2, b) 0.4, c) 0.6, d) 0.8.

With the aid of the waveforms in Fig. 4.3, the 3-level inductor duty cycle D_{Ind_3L} is represented in terms of switching duty cycle as follows:

$$D_{Ind\_3L} = \frac{T_{On\_Ind}}{T_{On\_Ind} + T_{Off\_Ind}} = \frac{T_{On\_Ind}}{T/2} = \begin{cases} 2D & 0 < D < 0.5 \\ 2D - 1 & 0.5 < D < 1 \end{cases} \quad (4.4)$$

However, the assumption of this analysis is not very accurate at D=0.5, as the 3-level converter operates in resonance mode and the inductor current waveform has a sinusoidal shape as in Fig. 4.4 and its peak-to-peak value is minimum but not zero.

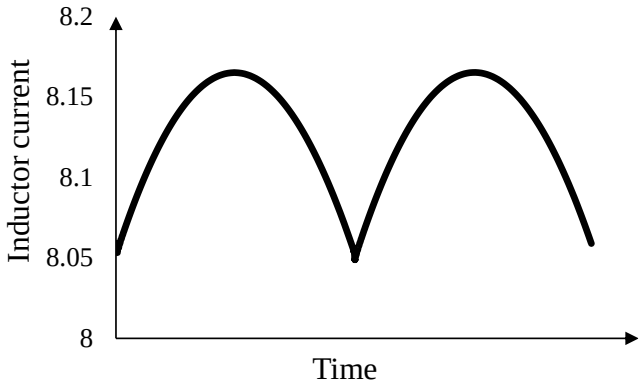


Fig. 4.4 3-level converter inductor current waveform of in a single switching cycle at D=0.5.

The switching duty cycle *D* in the interleaved buck ripple reduction formula presented by [80] is replaced with (4.4). Hence, the multiphase interleaved 3-level output ripple reduction formula becomes as in (4.5) and plotted in Fig. 4.5.

$$\Delta I_{Nph\%\_3L} = \frac{\Delta I_{Nph\_3L}}{\Delta I_{Ph\_3L}} = \frac{N_{Ph}}{D_{Ind\_3L}(1 - D_{Ind\_3L})}\left(D_{Ind\_3L} - \frac{m}{N_{Ph}}\right)\left(\frac{1+m}{N_{Ph}} - D_{Ind\_3L}\right) \quad (4.5)$$

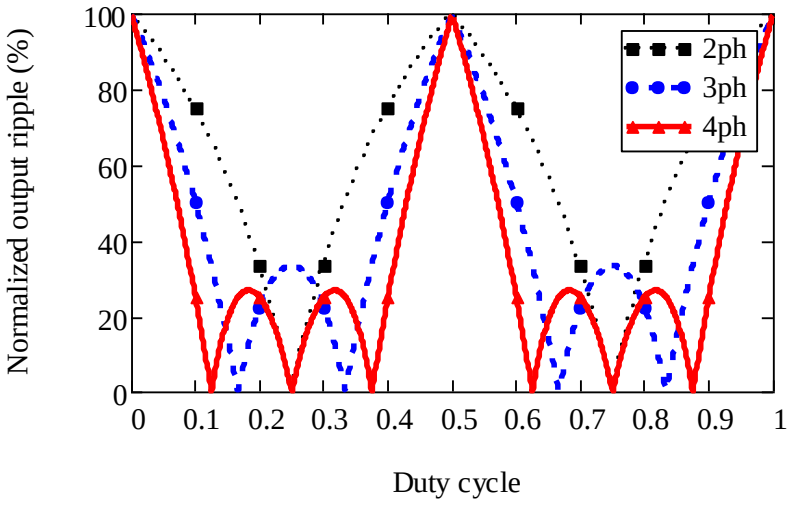


Fig. 4.5 Multiphase interleaved 3-level normalised output current ripple.

Similar to multiphase buck, phase current ripple is limited below a maximum value so that the overall current ripple can be recalculated accordingly. Then phase inductance L_{Ph_3L} is calculated considering previous assumptions as follows:

$$L_{Ph\_3L} = \begin{cases} \dfrac{(0.5 - D)V_{OUT}}{\Delta I_{ph\%\_3L}\, I_{Ph\_dc}\, F_{SW}} & 0 \le D < 0.5 \\ \dfrac{(-D^2 + 1.5D - 0.5)\dfrac{V_{OUT}}{D}}{\Delta I_{ph\%\_3L}\, I_{Ph\_dc}\, F_{SW}} & 0.5 \le D < 1 \end{cases} \tag{4.6}$$

The inductor peak stored energy indicates its size and is calculated as:

$$E_{L\_PK} = \frac{1}{2} N_{Ph} L_{Ph\_3L} {I_{Ph\_PK}}^2 \tag{4.7}$$

where I_{Ph_PK} is the peak phase current.

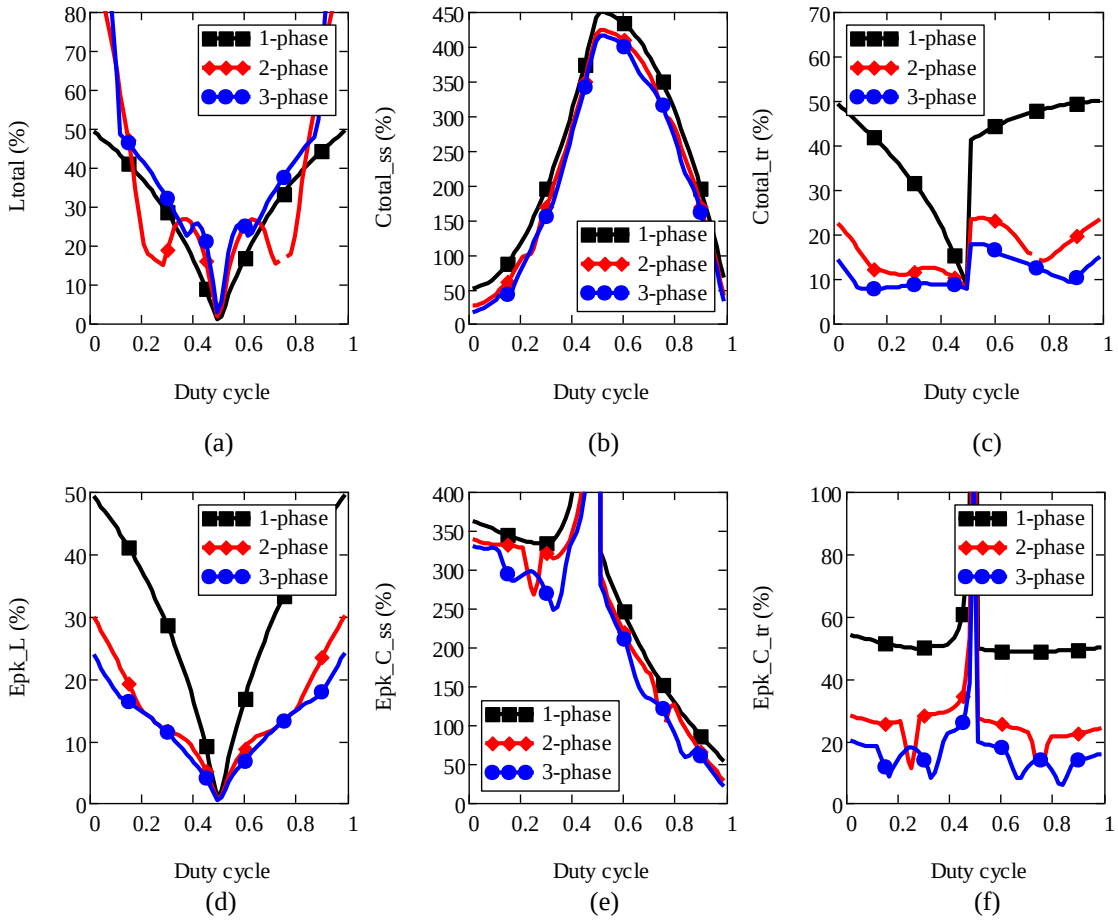


Fig. 4.6 Multiphase 3-level passives analysis normalised to single-phase buck.

Similar to multiphase buck, the total inductances and inductor peak energies for the 3-level with various numbers of phases, normalised to a single-phase basic buck converter,

are shown in Fig. 4.6(a, d). It shows that the 3-level significantly reduces inductor peak energy but increasing N_{Ph} is not noticeably beneficial beyond a 2-phase configuration. It also shows a better reduction in inductor energy than the multiphase buck, as the multiphase buck inductor energy was clipped at 40% approximately in Fig. 4.2(d). The 3-level topology is not impacted by limiting the ΔI_{Ph_3L} maximum value as a single-phase is capable of reducing ΔI_{Ph_3L} up to zero at D = 0.5.

4.3.2 *Output capacitance selection*

Steady-state output capacitance $C_{OUT\_3L\_SS}$ is calculated in (4.8), the same as the buck converter but with double the switching frequency F_{SW} and the total output current ripple ΔI_{Nph_3L} of the multiphase 3-level converter.

$$C_{OUT\_3L\_SS} = \frac{\Delta I_{Nph\_3L}}{16 N_{Ph} F_{Sw} \Delta V_{Out}} \tag{4.8}$$

Load transient output capacitance $C_{OUT\_3L\_Tr}$ is calculated in (4.9) as in [108] for loading and unloading transient conditions assuming fixed F_{SW} and with the buck duty cycle replaced by D_{Ind_3L}, as in (4.4) during the controller delay (reaction) time.

$$C_{OUT\_3L\_Tr} = \begin{cases} \dfrac{N_{Ph} L_{Ph\_3L} {I_{Ph\_dc}}^2}{2 V_{OS} V_{OUT}} & loading \\ \dfrac{I_{Ph\_dc}(1 - D_{Ind\_3L})}{V_{OS} F_{SW}} + \dfrac{N_{Ph} L_{Ph\_3L} {I_{Ph\_dc}}^2}{2 V_{OS} (V_{IN} - V_{OUT})} & unloading \end{cases} \tag{4.9}$$

4.3.3 *Flying capacitance selection*

The 3-level converter has a flying capacitor per phase C_{Fly} which is calculated as in [109]:

$$C_{Fly} = \begin{cases} \dfrac{D^2}{0.5 \alpha N_{Ph} R_{load} F_{SW}} & 0 \le D < 0.5 \\ \dfrac{D(1 - D)}{0.5 \alpha N_{Ph} R_{load} F_{SW}} & 0.5 \le D < 1 \end{cases} \tag{4.10}$$

where α is the desired voltage ripple across the capacitor, i.e. the excessive stress on the switches. The average voltage across the flying capacitor is V_{IN}/2, and its peak energy is calculated as:

$$Epk_{Cfly\_3L} = N_{Ph} 0.5\, C_{fly} (0.5 V_{IN} (1 + \alpha))^2 \tag{4.11}$$

The total capacitance in the multiphase 3-level converter for steady-state (C_{Total_SS} = $C_{OUT\_3L\_SS}$ + C_{Fly}) and load transient requirements (C_{Total_Tr} = $C_{OUT\_3L\_Tr}$ + C_{Fly}), are presented in Fig. 4.6(b, c) respectively normalised to a single-phase buck. It shows high C_{Total_SS} values, which are determined mainly by C_{Fly} value as it is much bigger than $C_{OUT\_3L\_SS}$ value. In contrast, there is a clear improvement in C_{Total_Tr}, a parameter that generally tends to dominate the selection of the capacitors.

The same trends are to be seen in the results of total peak capacitor energy (calculated as $Epk_{Ctot\_3L} = Epk_{Cout\_3L} + Epk_{Cfly\_3L}$) in Fig. 4.6(e, f) for steady-state and load transient requirements, respectively. Normalised results in Fig. 4.6(e, f) are not applicable at D = 0.5 as the 3-level converter has theoretically zero current ripple at this operating point.

Comparing the results of Fig. 4.2 and Fig. 4.6 shows that the multiphase 3-level has a better reduction in inductor energy than a multiphase buck. In terms of capacitance, it requires much higher steady-state capacitance due to the added flying capacitance per phase; however, the overall capacitance for load transient requirements is close to the multiphase buck to some extent. The differences will be addressed in the converter design section.

4.4 *Two-phase coupled inductor*

4.4.1 *Multiphase buck*

The 2-phase coupled inductor was discussed for the multiphase buck converter in chapter 3, which presented formulas for steady-state and transient inductances. Normalised steady-state inductance is mentioned again in (4.12) for reference.

$$L_{SS\_B\_norm} = \frac{L_{SS}}{L_{Self}} = \begin{cases} \dfrac{1 - {k_f}^2}{1 + \dfrac{D k_f}{1 - D}} & 0 \le D < 0.5 \\ \dfrac{1 - {k_f}^2}{1 + \dfrac{(1 - D) k_f}{D}} & 0.5 \le D < 1 \end{cases} \tag{4.12}$$

where k_f is the coupling factor.

Formulas for coupling factor at a given value of $L_{SS\_B\_norm}$, and the coupling factor that maximises $L_{SS\_B\_norm}$ were discussed in chapter 3; these are represented in Fig. 4.7 again for reference.

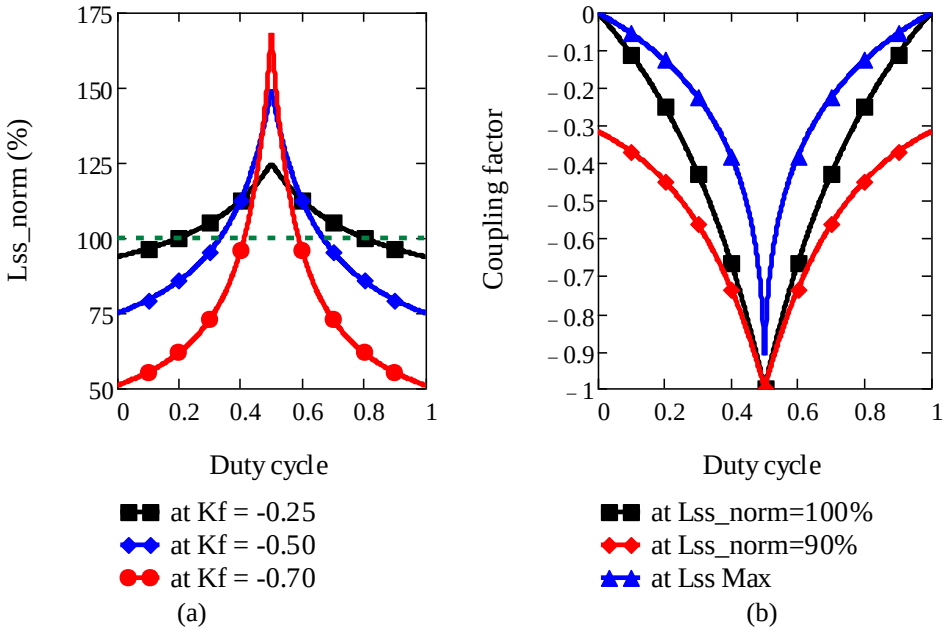


Fig. 4.7 2-phase coupled inductor analysis in multiphase buck topology, (a) $L_{SS\_B\_norm}$ vs duty cycle at different k_f values, (b) k_f vs duty cycle at different $L_{SS\_B\_norm}$ conditions.

4.4.2 *Multiphase 3-Level*

The 3-level converter operates in two modes, for $0 < D \leq 0.5$ and $0.5 \leq D < 1$, as illustrated in [109], resulting in two modes of the inductor current duty cycle as in (4.4), in addition to the two modes of the coupled inductor vs. duty cycle as explained in [79]. The normalised steady-state phase inductance $L_{SS\_3L\_norm}$ is derived by replacing the duty cycle in the inductance formulas in [79] with that for the 3-level duty cycle from (4.4). This combination means that the coupled inductor in a 2-phase 3-level interleaved converter operates in four modes as illustrated in Fig. 4.8 and presented in the derived formula in (4.13). In contrast, the different operating modes do not affect the transient inductance in (4.14).

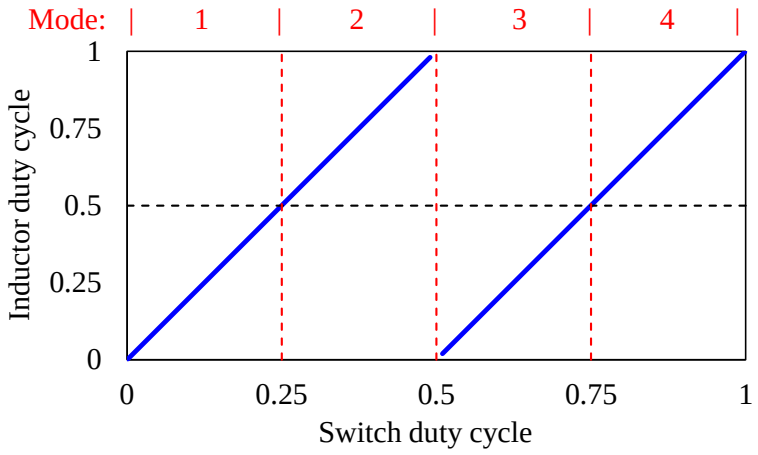


Fig. 4.8 Illustration of the four modes of the 2-phase coupled inductor in 3-level converter.

$$L_{SS\_3L\_norm} = \frac{L_{SS}}{L_{Self}} = \begin{cases} \dfrac{1-{k_f}^2}{1+\dfrac{2Dk_f}{1-2D}} & 0 < D < 0.25 \\ \dfrac{1-{k_f}^2}{1+\dfrac{(1-2D)k_f}{2D}} & 0.25 < D < 0.5 \\ \dfrac{1-{k_f}^2}{1+\dfrac{(2D-1)k_f}{2-2D}} & 0.5 < D < 0.75 \\ \dfrac{1-{k_f}^2}{1+\dfrac{(2-2D)k_f}{2D-1}} & 0.75 < D < 1 \end{cases} \tag{4.13}$$

$$L_{Tr\_3L\_norm} = \frac{L_{Tr}}{L_{Self}} = 1 + k_f \tag{4.14}$$

The steady-state phase inductance is related to the peak-to-peak phase current ripple ΔI_{Ph_3L}. The analysis of $L_{SS\_3L\_norm}$ in (4.13) is plotted at different negative coupling factor, K_f, values in Fig. 4.9(a). It shows inductance enhancement around D = 0.25 & 1.0 for a narrow range; however, the multiphase buck has inductance enhancement around D = 0.5. These results show a conflict between optimum conditions of the coupled inductor at D = 0.25 & 1 and the interleaved 3-level topology at D = 0.5. However, this analysis is generic and helps to identify the suitable coupling factor for effective converter operation at any range of duty cycle.

Coupling factor is analysed at a given value of $L_{SS\_3L\_norm}$ = x in the multiphase 3-level converter and expressed in (4.15), similar to the coupling factor analysis of $L_{SS\_B\_norm}$ in the multiphase buck, presented in chapter 3. The coupling factor at the maximum $L_{SS\_3L\_norm}$ trajectory is found by solving $\frac{d}{dk_f} L_{SS\_3L\_norm} = 0$, and it is expressed in (4.16).

$$K_f(x, D) = \begin{cases} \dfrac{xD + \sqrt{D^2(x^2-4x+4) + 4D(x-1) - x + 1}}{2D-1} & 0 < D < 0.25 \\ \dfrac{2xD - x - \sqrt{D^2(4x^2-16x+16) + x^2(1-4D)}}{4D} & 0.25 < D < 0.5 \\ \dfrac{2xD - x + \sqrt{D^2(4x^2-16x+16) - 4D(x^2-8x+8) + x^2 - 16x + 16}}{4(D-1)} & 0.5 < D < 0.75 \\ \dfrac{x(D-1) - \sqrt{D^2(x^2-4x+4) + x^2(1-2D) + 4D(x-1) - x + 1}}{2D-1} & 0.75 < D < 1 \end{cases} \tag{4.15}$$

$$K_{f\_3L\_Lmax} = \begin{cases} \dfrac{2D-1+\sqrt{1-4D}}{2D} & 0 < D < 0.25 \\ \dfrac{2D-\sqrt{4D-1}}{2D-1} & 0.25 < D < 0.5 \\ \dfrac{2D-2+\sqrt{3-4D}}{2D-1} & 0.5 < D < 0.75 \\ \dfrac{2D-1+\sqrt{4D-3}}{2D-2} & 0.75 < D < 1 \end{cases} \tag{4.16}$$

In Fig. 4.9(b), the coupling factor is plotted for $L_{SS\_3L\_norm}$ = 1, 0.9 and at the maximum $L_{SS\_3L\_norm}$ value trajectory. This provides a design guideline for coupling factor selection for a typical converter specification with a wide duty cycle range. The smallest coupling value should be chosen over the operating duty cycle range to ensure the converter operates effectively and avoids inductance roll-off under all operating conditions.

This analysis of the multiphase 3-level converter with a 2-phase coupled inductor is generic and helps identify the suitable coupling factor for other applications.

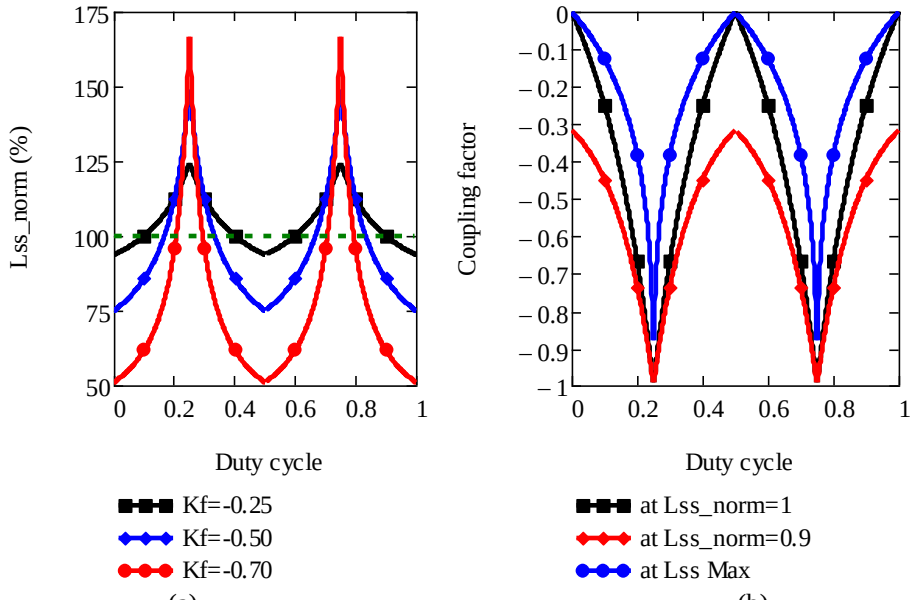


Fig. 4.9 2-phase coupled inductor analysis in multiphase 3-level topology, (a) $L_{SS\_3L\_norm}$ vs duty cycle at different k_f values, (b) k_f vs duty cycle at different $L_{SS\_3L\_norm}$ conditions.

4.5 *Converter design study*

4.5.1 *Passive components: multiphase 3-level vs multiphase buck*

Based on the presented analysis in the previous sections, passive components are evaluated for the converter specifications listed in Table 4.1. These specifications are typical for a Point-of-Load (POL) step down converter; they are also suitable for applications of the first stage of a two-stage conversion to <1 V output voltage. The

analysis accounts for a 200% maximum limit of phase current ripple at full load to prevent negative phase current. For these specifications, the duty cycle ranges from 0.27 to 0.72, assuming ideal components. For comparison purposes, a similar analysis is applied for the multiphase buck topology.

Table 4.1 Converter design specifications.

Symbol	Quantity	Value	Unit
F_{SW}	Switching frequency	20	MHz
V_{IN}	Input voltage	2.5 – 6.6	V
V_{OUT}	Output voltage	1.8	V
I_{DC}	Output DC current	3	A
ΔI_{Nph}	Output current ripple	0.75 (25%)	A
ΔV_{OUT}	Output voltage ripple	90 (5%)	mV
V_{OS}, V_{US}	V_{OUT} overshoot, undershoot	90 (5%)	mV
I_{Low} to I_{High}	Load transient	0 to 3	A

The design procedure for the converters is summarised in Fig. 4.10. The procedure starts by setting the converter specifications, then ΔI_{Ph} is calculated at each N_{Ph} value and maintained at $\leq 2I_{Ph\_DC}$. Then other parameters are calculated, mainly L_{Ph}, which is required to calculate I_{Ph_PK}, E_{L_PK} and C_{Out_Tr}. L_{Ph} and k_f calculations are required for the inductor design in the next section. Then ΔI_{Nph} value is updated to get its maximum value to estimate C_{Out_SS}. The output voltage ripple ΔV_{OUT} is then updated according to the selected output capacitance, which is required to calculate the capacitors' peak energy.

This procedure with phase current ripple limit consideration is a practical way for component selection. During this procedure, some parameters are a function of the duty cycle, so the maximum value is calculated over the duty cycle range and selected as $max\{f(D), D \in [D_{Min} \sim D_{Max}]\}$.

Passive components analysis for the converter specification listed in Table 4.1 is shown in Fig. 4.11. In Fig. 4.11(a), the total inductance required for the 3-level increases above 2-phases because of limiting the maximum phase current ripple to 200%. However, the inductor peak energy in Fig. 4.11(d) saturates close to a minimum value at N_{ph} = 2, meaning that adding extra phases does not necessarily result in reduced inductor size. Compared with the multiphase buck in Fig. 4.11(a, d), the multiphase 3-level has significantly less total inductance and inductor peak energy. The potential for air-core

PCB inductor size-reduction corresponding to Fig. 4.11 is investigated in the inductor design section.

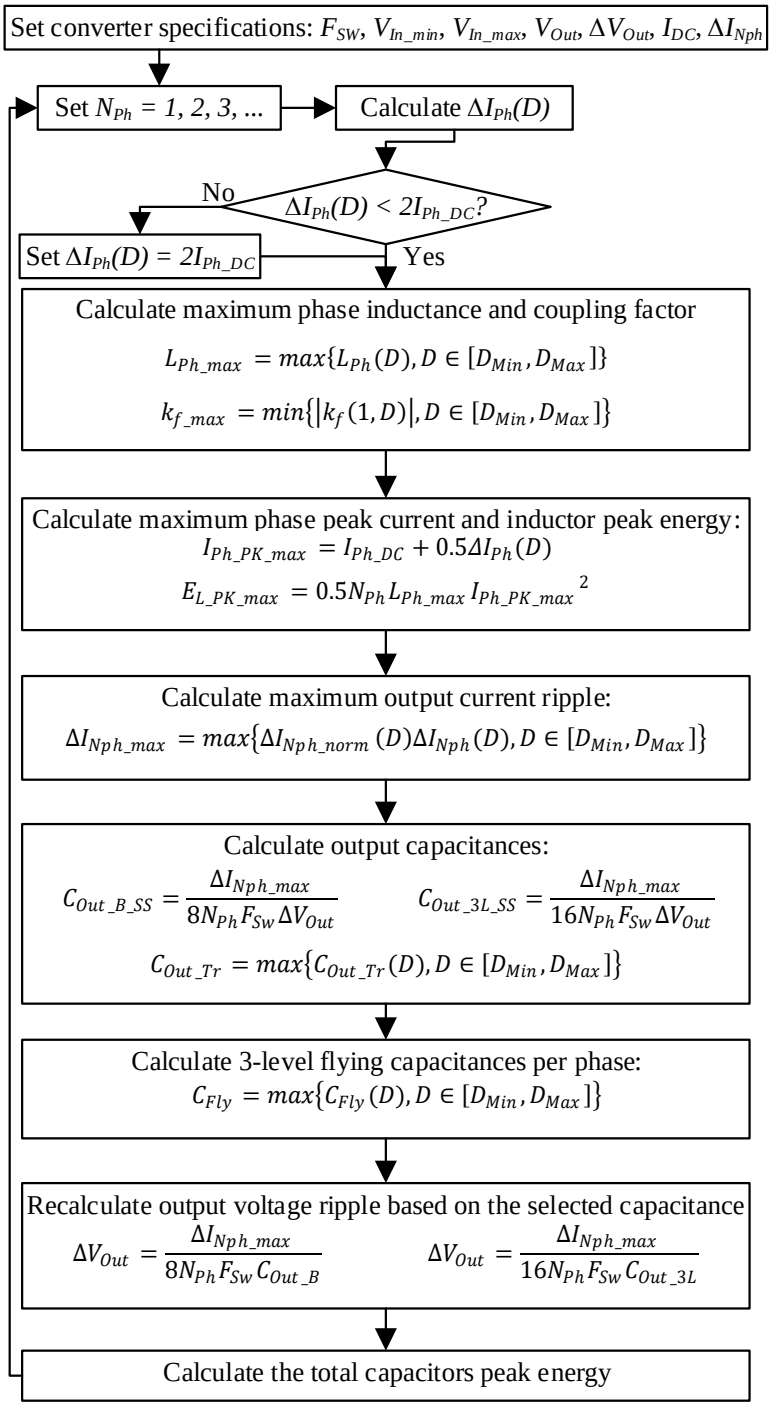


Fig. 4.10 Passives' selection procedure of multiphase buck and 3-level converters.

The steady-state total output capacitance and corresponding peak energy are shown for reference in Fig. 4.11(b, e), respectively. However, the capacitance for load transient requirements is much higher hence more important. The total capacitance for load transient and corresponding peak energy are shown in Fig. 4.11(c, f). The reduction of

both also saturates close to a minimum value at N_{Ph} = 2. However, it indicates that the multiphase buck is better in reducing the capacitors' total peak energy in general.

Results in Fig. 4.11(d, f) for the inductors' and capacitors' total peak energy highlight the theoretical trade-offs between the multiphase buck and multiphase 3-level topologies. The multiphase buck requires lower capacitor energy, while the multiphase 3-level requires lower inductor energy. However, considering manufacturing technology limitations, reducing the passives' peak energy may not reach the goal of reducing passive components' actual volume. Note that inductor peak energy is more applicable to the cored inductors, which may be limited by saturation.

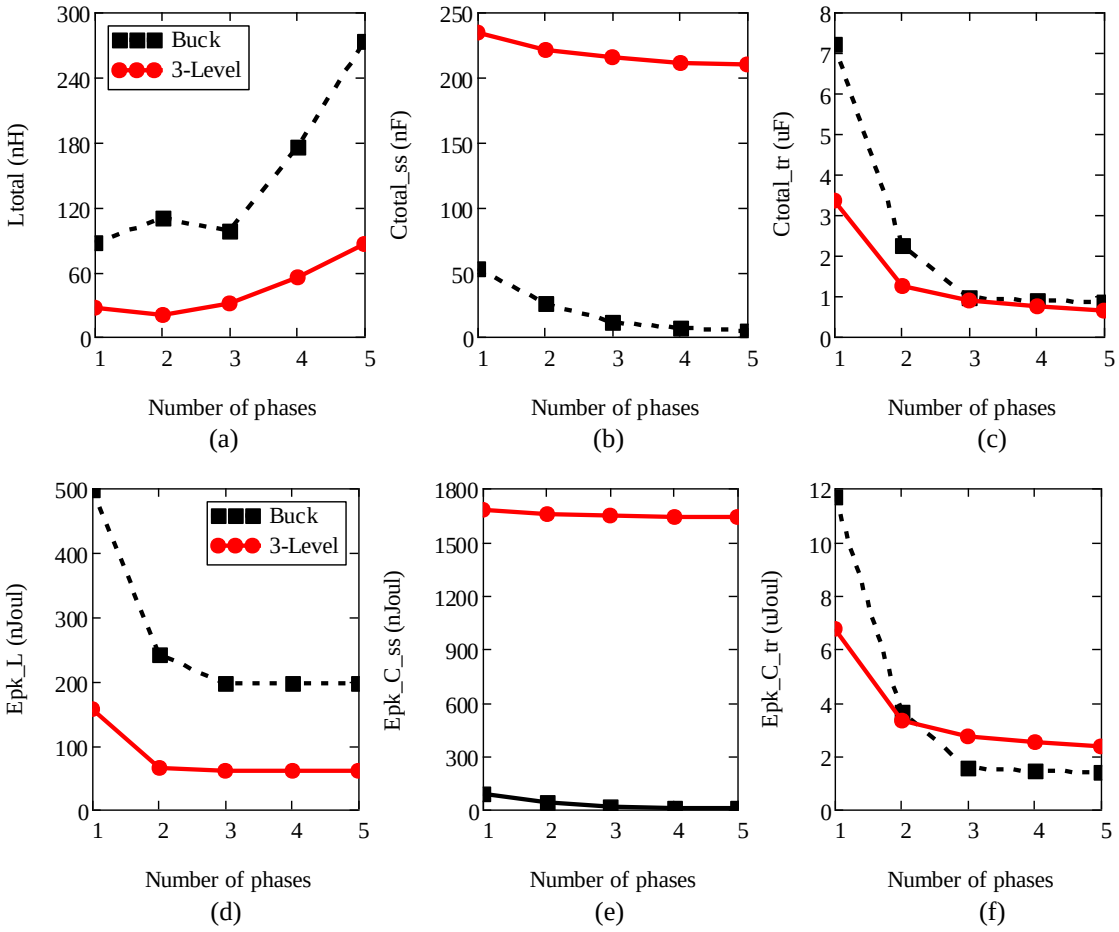


Fig. 4.11 Design study passive components in multiphase 3-level vs multiphase buck.

As for commercial MLCC capacitors, a wide range of capacitance and voltage ratings can fit in the same footprint area with minimal differences in capacitor height. On the other hand, for the considered PCB inductors, PCB manufacturing places limitations on minimum conductor dimensions, spacing, via diameter, and via-to-via spacing. This means the actual inductor volume may not follow the relative trend in inductor peak

energy predicted in Fig. 4.11(d). Instead, the actual inductors volume will increase again at some point vs. the number of phases where manufacturing technology is at its limits; this is the same issue as presented for the solenoid inductor case in chapter 3.

In terms of coupled inductors for the specifications in Table 4.1, applying the results of Fig. 4.9(b) over the operating duty cycle range shows that coupling is not recommended to maintain an effective steady-state inductance ≥ 100%. However, the coupling is more suitable for a 3-level converter operating around $D = 0.25$.

4.5.2 *Passive Components Selection for the Design Study*

Five configurations are selected to investigate the converter performance, i.e., 1, 2 & 4 phase buck and 1 & 2 phase 3-level. The required passive components to meet the given specifications are calculated and listed in Table 4.2.

Commercial capacitors are chosen in

Table 4.3 based on load transient capacitance requirements. The selected combination of the output capacitors is made to achieve a total impedance ≤ the target load-transient impedance Z_{Target}, calculated in (4.17), for frequencies ranging from the output ripple frequency (F_H) to the lower band frequency (F_L), calculated in (4.18).

$$Z_{Target} = \frac{V_{OS}}{I_{High} - I_{Low}} = \frac{90mV}{3A} = 30m\Omega \tag{4.17}$$

$$F_L = \sqrt{F_{LC}F_{ESR}} = \sqrt{\frac{1}{2\pi\sqrt{L_{Ph}C_{out}}}\frac{1}{2\pi C_{out}ESR}} \tag{4.18}$$

where ESR is the output capacitor series resistance, which is assumed initially as 3 mΩ to calculate the F_{LC} value; F_{LC} is the resonance frequency of the phase output filter. Then F_{LC} is used while choosing the commercial capacitors.

AC SPICE simulation of the commercial output capacitors' impedance vs frequency is presented in Fig. 4.12. It shows the combined capacitors' impedance below Z_{Target} over a wide frequency range for all cases. The comparison of the total capacitor area in

Table 4.3 correlates with the predictions of the capacitor energy in Fig. 4.11(f) to a good degree.

Table 4.2 Selected design cases.

Parameter	1-Ph Buck	2-Ph Buck	4-Ph Buck	1-Ph 3-Level	2-Ph 3-Level
L_{Ph} (nH)	87.3	54.6	43.6	27.3	10.3
L_{Total} (nH)	87.3	109.1	174.6	27.3	20.6
C_{Fly} (nF)	-	-	-	208.4	104.2
C_{OUT_SS} (nF)	52.1	26.1	6.2	26.1	13.1
C_{OUT_Tr} (uF)	7.22	2.24	0.9	3.16	1.03
C_{Total_SS} (nF)	52.1	26.1	6.2	234.5	221.5
C_{Total_Tr} (uF)	7.22	2.24	0.9	3.37	1.24
E_{Peak_L} (nJoul)	497.2	240.7	196.4	155.5	64
$E_{Peak\_C\_SS}$ (nJoul)	84.5	42.31	10.1	1676	1655
$E_{Peak\_C\_Tr}$ (uJoul)	11.7	3.63	1.46	6.8	3.3
2-Ph K_{f_max}	-	-0.375	-0.375	-	0

Table 4.3 Proposed commercial capacitors selection.

Converter	Capacitor	Part no.	Capacitance (uF)	Total area (mm^2)
1-Ph Buck	Cout	1x GCJ32ER91C685KE01 1x LLL219R71C224MA01 1x GRM155C80J474KE19	6.8 0.22 0.47	10.5
2-Ph Buck	Cout	1x GCM21BL8EG225KE07 1x LLL315R71C104MA11 1x GCM188R71H224KA64	2.2 0.1 0.22	7.62
4-Ph Buck	Cout	1x GCM21BR7YA684KA55 3x LLL153C80J104ME01	0.68 0.1	4
1-Ph 3-Level	Cout Cfly	2x GCM21BL8EG225KE07 2x LLL185C70G224MA11 1x LLL219R71C224MA01	2.2 0.22 0.22	10.06
1-Ph 3-Level	Cout Cfly	2x LLL219R71A474MA01 3x LLL153C80J104ME01 1x GCM188R71E154KA37	0.47 0.1 0.15	7.78

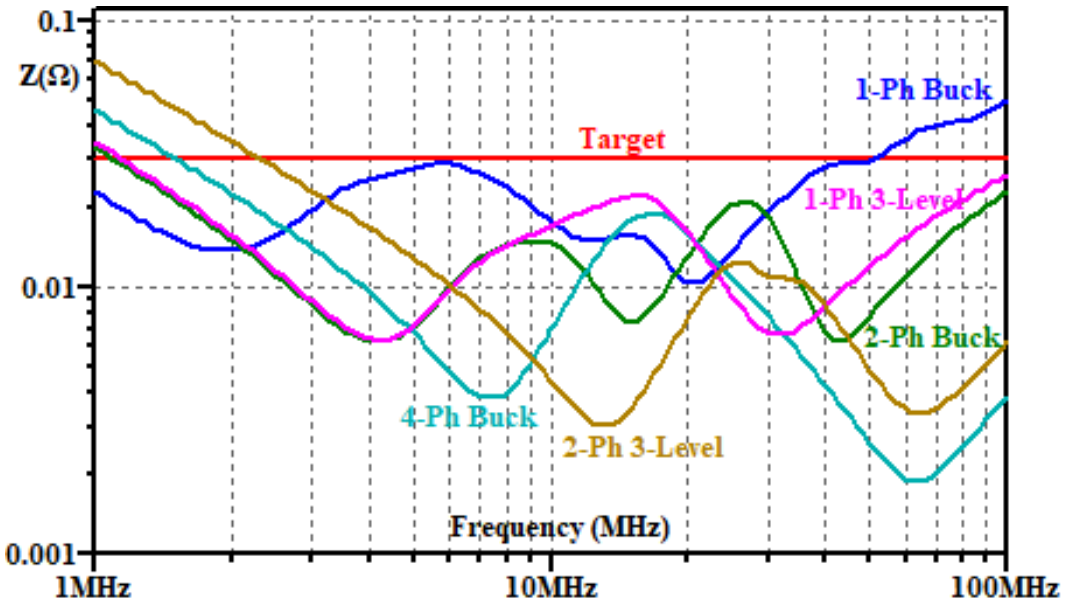
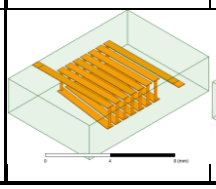
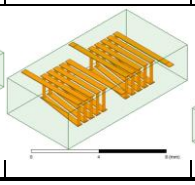
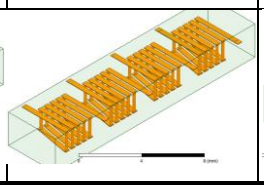
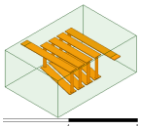
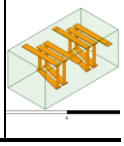


Fig. 4.12 Spice simulation of the commercial output capacitors impedance selected for the design studies.

4.6 *PCB inductor design*

For the converter design study, an air-core solenoid design integrated into a 2-layer FR4 PCB is considered. Hence, the size comparison is not affected by magnetic core saturation. Only the solenoid inductor is used in this chapter as its Q-factor per footprint area is better than the spiral inductor, as seen in chapter 3. The inductor design is based on PCB manufacturing constraints, i.e. copper thickness of 35 µm, PCB height of 1.6 mm, via diameter of 0.2 mm, minimum copper trace width and spacing of 0.15 mm, via annular ring of 0.125 mm, and minimum solder mask width of 0.07 mm. The conductor width is calculated based on the standard IPC-2221A [87] for a temperature rise of 50^{O}C at the maximum inductor RMS current. The choice of 50^{O}C is set as a reference point for this design study; however, future work will consider lower temperature rise. The inductor design follows the same procedures as described in chapter 3 and Appendix B. Inductor designs and FEA simulation results in Table 4.4 show the potential of the 3-level converter in reducing the inductor volume. As for the same number of switches, the inductor size of the single-phase 3-level is only 40% of the 2-phase buck inductor volume.

Table 4.4 Selected inductors' designs.

	Design	1-Ph Buck		2-Ph Buck		4-Ph Buck		1-Ph 3-Level		2-Ph 3-Level	
Calculations	L_{Ph} (nH)	87.7		55.1		44.1		27.6		10.5	
	R_{DC} (mΩ)	77.7		57.7		48.4		29.8		16.0	
	Q_{DC}	141.9		119.9		114.5		232.6		165.7	
	Area (mm^2)	26.5		10.9		9.0		10.0		3.1	
	Volume (mm^3)	42.5		17.5		14.5		16.0		4.9	
	Total Area*	26.5		25.5		45.3		10.0		8.3	
	Total Volume*	42.5		40.9		72.4		16.0		13.2	
FEA	Freq (MHz)	1	20	1	20	1	20	1	40	1	40
	L_S (nH)	92.3	90.7	55.9	54.8	46.3	45.2	32.4	31.6	13.3	12.9
	R_S (mΩ)	86.4	127.4	63.0	97.0	53.3	83.2	34.8	59.5	18.8	34.7
	Q at F_{SW}	134	89.5	112	71.0	109	68.3	117	66.8	89	46.6
FEA model											

* Multiphase inductors overall area and volume accounts for 1 mm spacing between inductors.

4.7 *Converter performance*

The converter simulation performance is investigated with the passives described in previous sections and a switcher based on EPC2040 GaN FET switches [93] for the high and low sides. Each FET connects to its gate driver through 1.9 and 1.3 Ω pull-up and pull-down resistors. The FETs are driven using the gate driver PE29102 [95], which is driven at 20 MHz using an FPGA development board.

With all the main components of the converters selected, considering non-coupled inductors, the estimated footprint areas are compared in Fig. 4.13. The gate driver area includes the area of the pull-up and pull-down resistors. It shows that the single-phase buck and 2-phase 3-level have very close footprint areas, but this may be because the switch and driver circuits are not optimal. However, the smallest inductor and total passives footprint areas were achieved by the 2-phase 3-level converter at the cost of circuit complexity.

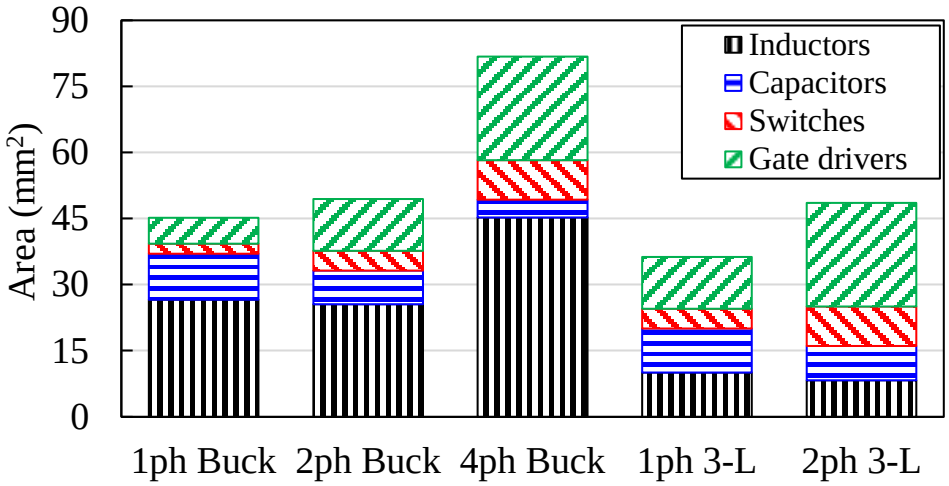


Fig. 4.13 Overall footprint area.

4.7.1 *Steady-state performance*

Open-loop circuit simulation is carried out using LTspice with spice models of EPC2040 switches for the high and low sides. To account for parasitic elements effects, the simulation model considers parasitic package inductance and resistance values of 20 pH and 1 mΩ, respectively, at each FET terminal. The deadtime was adjusted at 1 ns to minimise switching loss.

The inductor efficiency vs. load in Fig. 4.14 shows the 2-phase 3-level inductor achieving the highest overall inductor efficiency. The converter efficiency excluding and including the gate driver loss vs load is presented in Fig. 4.15 and Fig. 4.16, respectively. The inclusion of the gate driver loss affects the efficiency of the 3-level converters more than the buck converters, as the 3-level has double the number of switches and drivers per phase. Fig. 4.15 shows the 2-phase 3-level has the best overall efficiency curve as its inductor loss is smaller than other converters. However, the gate driver loss significantly affected the lighter load efficiency, as in Fig. 4.16.

Considering the combination of the efficiency curve and components' total area, the single-phase 3-level and 2-phase buck converters look more competitive than the others. In contrast, the 4-phase buck with the largest area is not competitive for these requirements. The 2-phase 3-level with the smallest inductors gives equal highest full load efficiency to the 2 and 4-phase buck with gate-driver loss included.

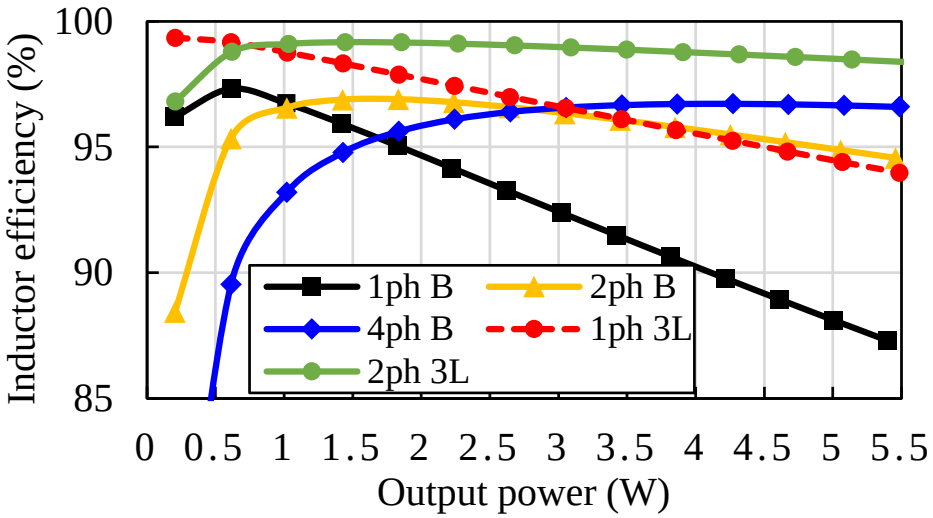


Fig. 4.14 Simulated inductor efficiency.

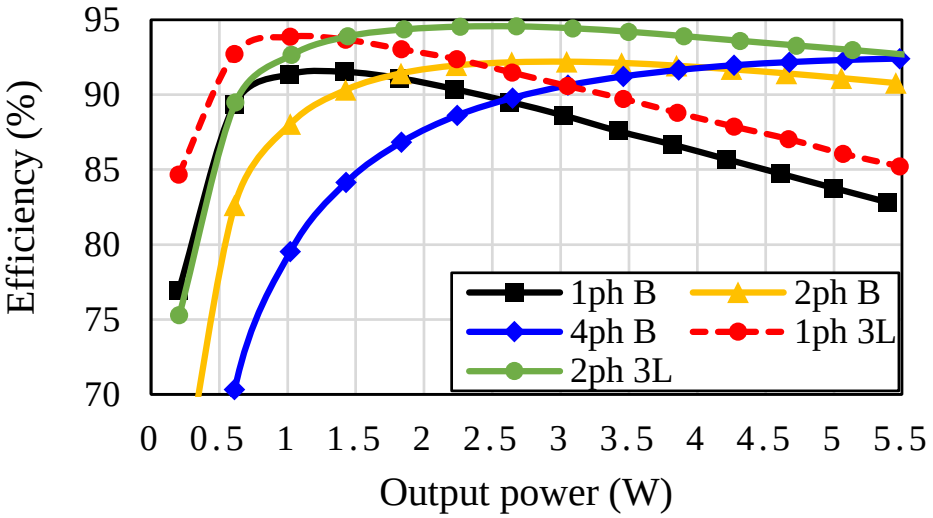


Fig. 4.15 Simulated converter efficiencies excluding gate driver loss.

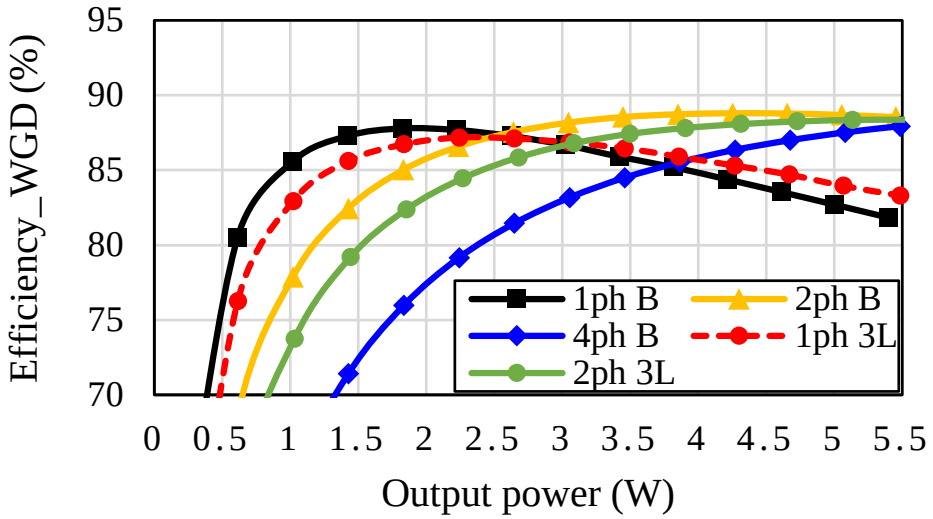


Fig. 4.16 Simulated converter efficiencies including gate driver loss.

4.7.2 *Closed-loop Load transient performance*

For an easier comparison of the load-transient performance of the five converters, a fixed ideal capacitance of 5 µF at the output in series with a 5 mΩ resistor was used in the simulation of the five converters. All converter models used a closed-loop controller with a Type 3 compensation network as in [111].

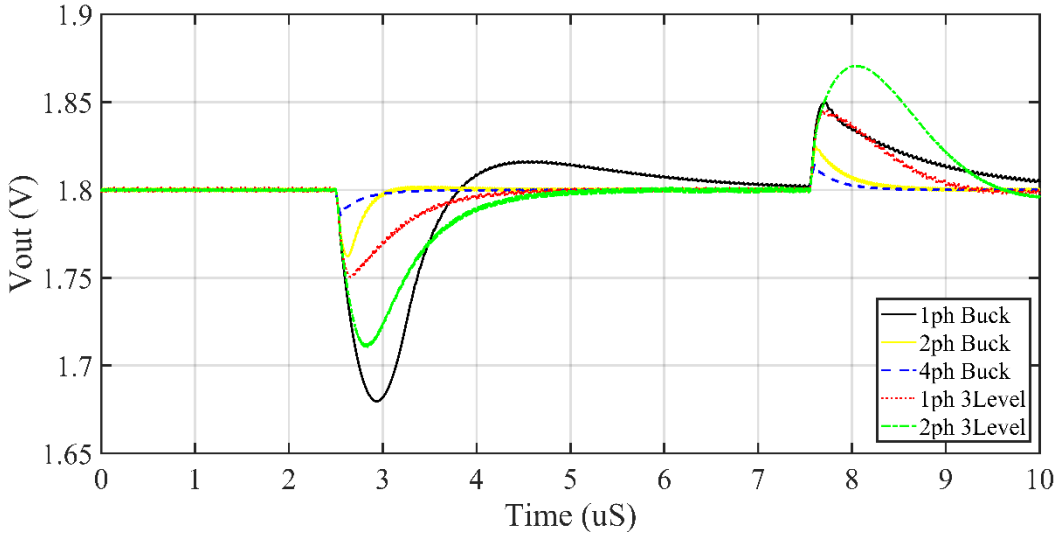


Fig. 4.17 Simulated load transient from 10% to 100% at V_{IN} = 4.5 V.

Results in Fig. 4.17 show the 4-phase buck with the best performance in terms of the overshoot and undershoot voltages and settling time; however, it has the biggest footprint area and poor efficiency curve, especially with gate driver loss included. Then the 2-phase buck converter comes next. The relative undershoot voltages with the fixed capacitance agree with the capacitor sizes in

Table 4.3, except for the 2-phase 3-level. The 2-phase 3-level shows overshoot and undershoot voltage values higher than expected compared to other converters; this will be investigated in future work.

4.8 *Summary*

This chapter presented passive components analysis in the multiphase interleaved 3-level converter topology and compared it against the multiphase interleaved buck topology in terms of total inductance, steady-state capacitance, load transient capacitance, and corresponding peak energy for these components. The analysis considered converter operation with wide input voltage specifications. The passive components comparison showed that the multiphase 3-level topology reduces inductor peak energy over the multiphase buck; however, it results in higher steady-state capacitor peak energy, as it

requires a flying capacitor per phase, although the required capacitors when considering load transients are smaller.

The coupled inductor characteristics were derived for a 2-phase inductor in multiphase 3-level topology. Guidelines were presented to select the coupling factor based on the converter specifications. It showed that the best operating point for exploiting coupling is at $D = 0.25$. However, from a circuit perspective, the best operating point is at $D = 0.5$, where a high coupling is not beneficial.

Five converter configurations were selected for the design study, for which recommended commercial capacitors were chosen, and air-core PCB integrated solenoid inductors were designed considering the manufacturing capabilities. The converters' steady-state efficiencies were examined through SPICE simulation. The results showed the significant effect of the gate driver losses, particularly on the 3-level converters. Closed-loop load transient performance was simulated with a fixed output capacitor, and it showed that multiphase buck performs better despite requiring larger inductors.

Chapter 5 – 4th Order Resonance Output Filter Topology

This chapter presents a novel design procedure for 4th order and 4th order resonance (4thRes) output filters, for given buck converter specifications, making components selection a straightforward process. An accurate filter analysis is provided to predict the filter component currents and voltages in both frequency and time domains. Application of the analysis in a design study of a 20 MHz, 5.4 W buck converter shows that the 4thRes filter has the potential to reduce the output passive components for a wide duty cycle range. As compared with a 2nd order filter at V_{IN} = 6.6 V to V_{OUT} = 1.8 V, total inductance, inductor energy, capacitance and capacitor energy are 58%, 35%, 45% and 31% lower, respectively. Air-core PCB integrated solenoid inductors are considered for implementation and testing within a prototype converter to show the impact of these filters on converter performance. The 4thRes filter achieved 3.7% and 3.6% higher full load efficiency than the 2nd and 4th order filters, respectively, and better load transient performance.

5.1 *Introduction*

Passive components in DC-DC converters occupy large volumes and contribute significantly to the overall converter loss, particularly the magnetic components. There are several ways to optimise the utilisation of magnetic components in terms of size or losses, like increasing the switching frequency, using a different converter topology, e.g. multiphase buck [13], [37], [84], using a different component structure and material, or using a higher order filter for better controlling the output voltage ripple [112]. A 4th-order filter, as in Fig. 5.1(b), provides twice the roll-off rate of a 2nd-order filter (Fig. 5.1(a)) and therefore has the potential for size reduction of the filter components to provide the same level of output voltage ripple.

While various benefits of high order filters have been reported in the literature, methods for filter design to achieve given DC-DC converter specifications within a minimum size have not been described. Furthermore, the performance of coupled inductors in high order filters has the potential for significantly reducing the filter size due to the high attenuation they produce through resonance with one of the filter capacitors. However, this has not

been fully exploited, partly because there is no detailed analysis available to enable the selection of suitable filter components. These gaps are addressed in this paper.

A design procedure for a 4th order low-pass filter for a DC-DC converter was introduced in [113]. The design procedure focused on increasing the converter bandwidth over a 2nd order filter (for an accelerator application) rather than on the size of the filter's passive components, where Butterworth, Bessel and critically damped filters were considered. The first inductance of the filter (*L1*) was designed based on the inductor current ripple. Then, a normalised filter transfer function was applied to determine the remaining filter components needed to achieve the required attenuation at the switching frequency.

In [114], the focus of filter design for a 100 W, 2-phase buck converter was on optimising an envelope tracking system to pass the envelope frequencies of 1.5 MHz and reject the 10 MHz switching harmonic frequencies rather than on minimisation of the passive component sizes. After reviewing the filtering performance for a number of 4th order filters, including Butterworth and Bessel, a Legendre-Papoulis was selected.

A fully integrated 450 MHz buck converter with a 4th order filter was demonstrated in [8] to have a similar area to a 2nd order filter of 0.4 mm^2; it was implemented with two side-by-side on-chip spiral air-core inductors. It was found that negative coupling (-0.05) due to the placement of the two inductors side-by-side provided greater attenuation than non-coupled at the switching frequency. This is a result of resonance between the mutual inductance and the first stage capacitor, as would be produced between L_3 and C_1 in the 4th-order resonance circuit (4thRes) of Fig. 5.1(c). However, neither the filter design nor the coupling factor was optimised to target given converter specifications.

A study in [115] investigated the coupled inductor as a filtering block for different applications. A 4th order filter with a coupled inductor was implemented and tested in a 50 kHz buck converter which showed 22 dB extra attenuation of the output ripple compared with a 2nd order filter. However, a size comparison was not presented, and the procedure for selecting filter components to achieve given DC-DC converter specifications was not described.

More studies considered high order filters in different circuit topologies and applications. A 42 kHz, 4 kW 4-phase buck converter with a 4th order filter and damping branch in each phase for a magnet power supply in a linear accelerator was described in [116]. A 500 W, 50 kHz buck converter with a 4th order filter was presented in [117], which

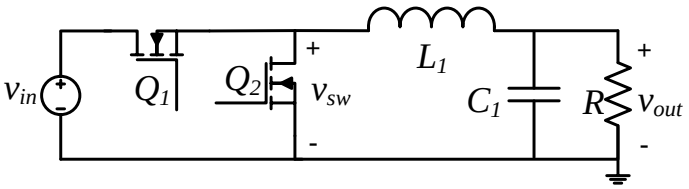
utilised the two filter stages to implement two feedback loops for fast envelope tracking. Most recently, a 0.21 W, 118 MHz integrated boost converter with an additional LC stage was presented in [118] to reduce the output ripple for analog applications. However, these studies do not focus on the impact of high order filters on the size of the passive components.

Therefore, this study provides a novel selection procedure for the passive components in 4th order and 4th order resonance (4thRes) output filters with a view to reducing their size for a given buck converter specification. The performance and size of the resulting filter components are benchmarked against those in a common 2nd order filter.

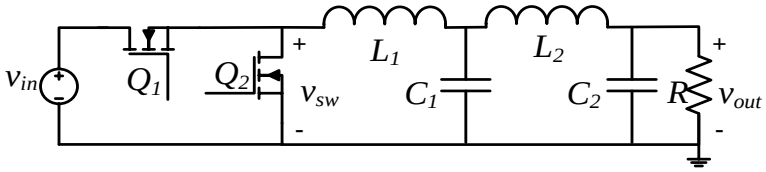
As mentioned, with a 4th order filter, there is an opportunity to implement the 3rd inductor, L_3, as the mutual inductance between L_1 and L_2. In this case, analysis of the proposed 4thRes filter using a non-coupled inductor is the first step toward component selection; then a coupled inductor can be used to achieve the same resonance feature. For simplicity, a Butterworth filter is chosen as a starting point for the filter design approach in this paper, but other standard filters could be applied.

The comparison is demonstrated for air-core PCB integrated inductors, where the target application is the first stage of a 2-stage step-down solution for Integrated Voltage Regulator (IVR) type loads powered by a wide input voltage battery source, e.g. as in [43], where stages 1 & 2 step down battery voltage from 3.8 to 1.5 V and then from 1.5 to 1 V respectively.

This chapter is based on our previous conference paper [119] and is structured as follows. Section 5.2 presents the filter design procedure for a standard 4th order low pass filter in terms of the specifications for a DC-DC buck converter. Then the same approach is applied for the 4thRes filter. Section 5.3 provides methods for accurately predicting the voltages and currents of the filter components in the frequency and time domains, so that they can be applied in passive component design. The filter design approach is employed to select passive components for a typical step-down buck converter specification, and these are compared against equivalent standard 2nd order low pass filter components in Section 5.4. Implementation of the required inductor designs in PCB is described in Section 5.5, and prototype inductor designs are compared for equivalent 2nd order, 4th order and 4thRes filters. Prototype converter testing and simulation results are presented and discussed in Section 5.6. Finally, conclusions are discussed in Section 5.7.



(a)



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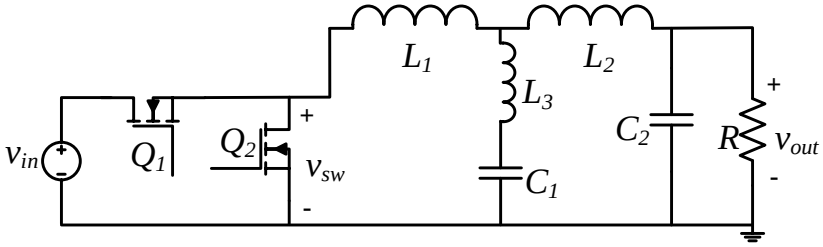


(c)

Fig. 5.1 (a) 2nd order filter, (b) 4th order filter, (c) 4th order resonance filter.

5.2 *Low pass filter design for a buck converter*

5.2.1 *Fourth-order low pass filter*

To analyse the filter components, the following transfer function is derived by circuit analysis of a 4th order filter as shown in Fig. 5.1(b):

$$G(s)_{4th} = \frac{v_{out}(s)}{v_{sw}(s)} = \frac{1}{X} \tag{5.1}$$

where

$$X = 1 + \left(\frac{L_1 + L_2}{R}\right)s + (C_1L_1 + C_2L_1 + C_2L_2)s^2 + \left(\frac{C_1L_1L_2}{R}\right)s^3 + (C_1C_2L_1L_2)s^4 \tag{5.2}$$

v_{sw} is the switching voltage, v_{out} is the output voltage, R is the load resistance, and L_1, L_2, C_1 & C_2 are the filter's inductive and capacitive elements shown in Fig. 5.1(b).

The transfer function in (5.1) is compared with the 4th order normalised filter transfer function, e.g. Butterworth filter:

$$G(s) = \frac{1}{1 + a_1\frac{s}{\omega_0} + a_2\frac{s^2}{{\omega_0}^2} + a_3\frac{s^3}{{\omega_0}^3} + a_4\frac{s^4}{{\omega_0}^4}} = \frac{1}{1 + A_1 s + A_2 s^2 + A_3 s^3 + A_4 s^4} \quad (5.3)$$

where a_1, a_2, a_3 & a_4 are the normalized filter parameters i.e. 2.613, 3.414, 2.613 & 1 respectively for a Butterworth filter [120], $A_n = a_n / \omega_0^n$ is used in (5.3) for simplicity, and ω_0 is the cut-off frequency.

By solving (5.1) and (5.3) together, we can get the four filter unknowns L_1, L_2, C_1 & C_2 in terms of the load resistor, R:

$$L_1 = RA_1 - \frac{R{A_3}^2}{A_2A_3 - A_1A_4} \quad (5.4)$$

$$L_2 = \frac{R{A_3}^2}{A_2A_3 - A_1A_4} \quad (5.5)$$

$$C_1 = \frac{(A_1A_4 - A_2A_3)^2}{RA_3\left(A_1A_2A_3 - {A_1}^2A_4 - {A_3}^2\right)} \quad (5.6)$$

$$C_2 = \frac{A_4}{RA_3} \quad (5.7)$$

ω_0 is chosen to achieve the required attenuation of the output voltage steady-state peak-to-peak ripple ΔV_{OUT} at the switching frequency $\omega_{SW} = 2\pi F_{SW}$. ΔV_{OUT} is specified at 5% for the first stage of a 2-stage regulator, where tighter regulation is provided by the second stage on-chip. Note also that in practice, additional output capacitance may be required to satisfy load transient requirements [121], over and above steady-state ripple filtering, but this is not considered at the initial design phase, where the objective is to assess the switching ripple filtering performances of the various filters. The effect of additional output capacitance for transient requirements considered in the measurements, in Section 5.6.

As an approximation, ω_0 is calculated assuming the gain of the highest order of the filter transfer function in (5.3) for each n^{th} harmonic as lower orders are negligible at frequencies > ω_0, i.e.:

$$G_n = \frac{\omega_0^4}{a_4 s^4} \quad \text{at} \quad s = jn\omega_{SW} \tag{5.8}$$

By assuming that ΔV_{OUT} of the filter is the summation of each harmonic amplitude multiplied by the filter gain at the corresponding frequency, then ΔV_{OUT} is represented as:

$$\Delta V_{OUT} = \sum_{n=1}^{Nh} |G_n \Delta V_n| \tag{5.9}$$

where N_h is the number of harmonics required to be attenuated, considering the first 10 harmonics is accurate enough for this study, and ΔV_n is the peak-to-peak amplitude of the n^{th} harmonic, which is calculated using Fourier analysis as follows:

$$\Delta V_n = \frac{4V_{OUT}}{n\pi D} \sin(n\pi D) \tag{5.10}$$

where D is the switching duty cycle.

By substituting (5.8) and (5.10) into (5.9), ΔV_{OUT} is found as:

$$\Delta V_{OUT} = \left(\frac{\omega_0}{\omega_{SW}}\right)^4 \frac{4V_{OUT}}{a_4 \pi D} \sum_{n=1}^{Nh} \frac{|\sin(n\pi D)|}{n^5} \tag{5.11}$$

As ΔV_{OUT} is a predetermined converter specification, then (5.11) is solved for ω_0 as follows:

$$\omega_0 = \omega_{SW} \sqrt[4]{\frac{\Delta V_{OUT}}{V_{OUT}} \frac{a_4 \pi D}{4 \sum_{n=1}^{Nh} \frac{|\sin(n\pi D)|}{n^5}}} \tag{5.12}$$

In this way, the filter attenuates the switching harmonics to the desired ΔV_{OUT} value at the output signal. This filter design approach for DC-DC converter always results in $L_1 > L_2$ and $C_1 > C_2$.

5.2.2 *Fourth-order resonance low pass filter*

In the proposed 4thRes filter (shown in Fig. 5.1(c)), the inductor L_3 resonates with the capacitor C_1. Its transfer function was derived using circuit analysis and is simplified to:

$$G(s)_{4th\_Res} = \frac{v_{out}(s)}{v_{sw}(s)} = \frac{1 + (C_1 L_3)s^2}{X_{Res}} \tag{5.13}$$

where

$$X_{Res} = 1 + \left(\frac{L_1 + L_2}{R}\right)s + (C_1L_1 + C_1L_3 + C_2L_1 + C_2L_2)s^2 + \left(\frac{C_1}{R}(L_1L_2 + L_1L_3 + L_2L_3)\right)s^3 + \left(C_1C_2(L_1L_2 + L_1L_3 + L_2L_3)\right)s^4 \quad (5.14)$$

The resonance of C_1 with L_3 makes a double zero in the transfer function, which is placed at the switching frequency to attenuate the first harmonic amplitude effectively. For frequencies below the double zero, the resonance filter response follows a 4th order characteristic, and afterwards, it follows a 2nd order characteristic, which makes the gain at the 2nd harmonic greater than the 1st harmonic. This will be considered in the selection of the cut-off frequency. The double zero is added to the normalised filter transfer function as follows:

$$G(s)_{4thRes\_norm} = \frac{1 + \frac{1}{\omega_{SW}^2}s^2}{1 + a_1\frac{s}{\omega_0} + a_2\frac{s^2}{\omega_0^2} + a_3\frac{s^3}{\omega_0^3} + a_4\frac{s^4}{\omega_0^4}} = \frac{1 + \frac{1}{\omega_{SW}^2}s^2}{1 + A_1s + A_2s^2 + A_3s^3 + A_4s^4} \quad (5.15)$$

By comparing (5.13) and (5.15), we can get from the denominator four equations with five unknowns, i.e., L_1, L_2, L_3, C_1 & C_2. One unknown is eliminated with the help of the numerator by placing the double zero at the switching frequency to give:

$$L_3 = \frac{1}{\omega_{SW}{}^2C_1} = \frac{1}{4\pi^2F_{SW}{}^2C_1} \quad (5.16)$$

Substituting (5.16) into (5.14) eliminates L_3, then (5.14) and the denominator of (5.15) are solved together to get:

$$L_1 = \frac{R\omega_{SW}{}^2\left(A_1{}^2A_4 - A_1A_2A_3 + A_3{}^2\right)}{A_3 + \omega_{SW}{}^2(A_1A_4 - A_2A_3)} \quad (5.17)$$

$$L_2 = \frac{RA_3(A_1 - A_3\omega_{SW}{}^2)}{A_3 + \omega_{SW}{}^2(A_1A_4 - A_2A_3)} \quad (5.18)$$

$$C_1 = \frac{\left(A_3 + {\omega_{SW}}^2(A_1A_4 - A_2A_3)\right)^2}{RA_3{\omega_{SW}}^4\left(A_1A_2A_3 - {A_1}^2A_4 - {A_3}^2\right)} \tag{5.19}$$

$$C_2 = \frac{A_4}{RA_3} \tag{5.20}$$

Similar to Section 5.2.1, ω_0 calculations assume the gain of the highest order of the filter transfer function in (5.15) for n[th] harmonic as follows:

$$G_n = \frac{1+\frac{s^2}{\omega_{SW}^2}}{\frac{a_4}{\omega_0^4}s^4} \quad \text{at} \quad s = jn\omega_{SW} \tag{5.21}$$

As equations (5.9) and (5.10) apply here as well, then (5.10) and (5.21) are substituted into (5.9) to express ΔV_{OUT} as follows:

$$\Delta V_{OUT} = \left(\frac{\omega_0}{\omega_{SW}}\right)^4 \frac{4V_{OUT}}{a_4\pi D}\sum_{n=1}^{Nh}\frac{|(1-n^2)\sin(n\pi D)|}{n^5} \tag{5.22}$$

Then (5.22) is solved for ω_0 as follows:

$$\omega_0 = {\omega_{SW}}^4\sqrt{\frac{\Delta V_{OUT}}{V_{OUT}}\frac{a_4\pi D}{4\sum_{n=1}^{Nh}\frac{|(1-n^2)\sin(n\pi D)|}{n^5}}} \tag{5.23}$$

The formulas (5.16) to (5.20) are used to determine the component values of the 4thRes filter in a buck converter. This filter design approach always results in $L_1 > L_2 > L_3$ and $C_1 > C_2$.

Fig. 5.2 shows a comparison between the calculated cut-off frequency in (5.12) and (5.23) at $\Delta V_{OUT}/V_{OUT} = 0.05$, assuming the 1[st] stage specification of a 2-stage converter as discussed above. It shows that ω_0 is higher for the 4thRes filter over the whole duty cycle range, which means it is expected to require smaller passive components than the normal 4[th] order filter and allow higher bandwidth of the closed-loop converter. However, closed-loop control is not within the scope of this study.

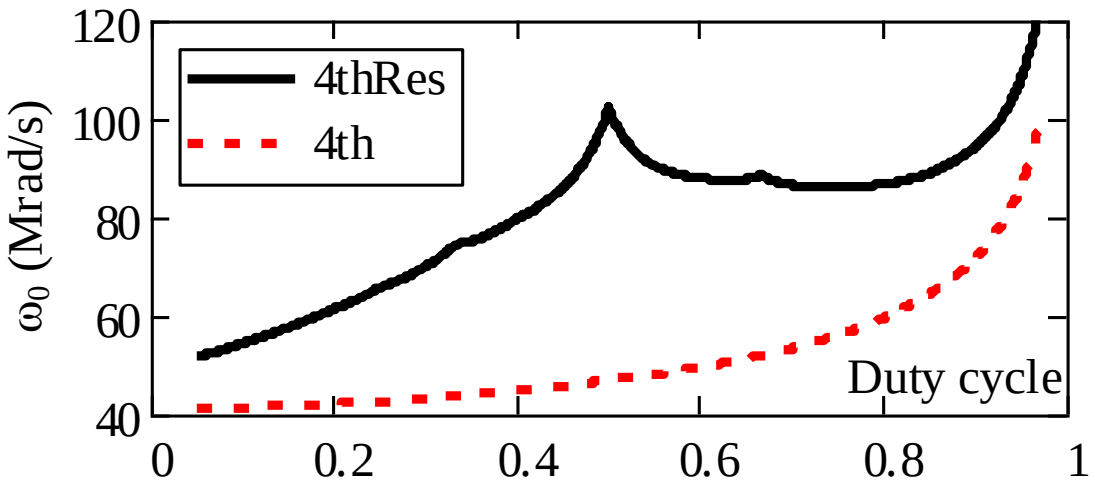


Fig. 5.2 Comparison of the calculated cut-off frequency at $\Delta V_{OUT}/V_{OUT} = 0.05$.

5.3 *Filter analysis*

In addition to filter component values, the filter size is determined by the voltages and currents carried by each filter component. To predict these voltages and currents, the output filter is first analysed in the s-domain, including the components' parasitic elements as detailed in Fig. 5.3, and the results are then translated to the time domain.

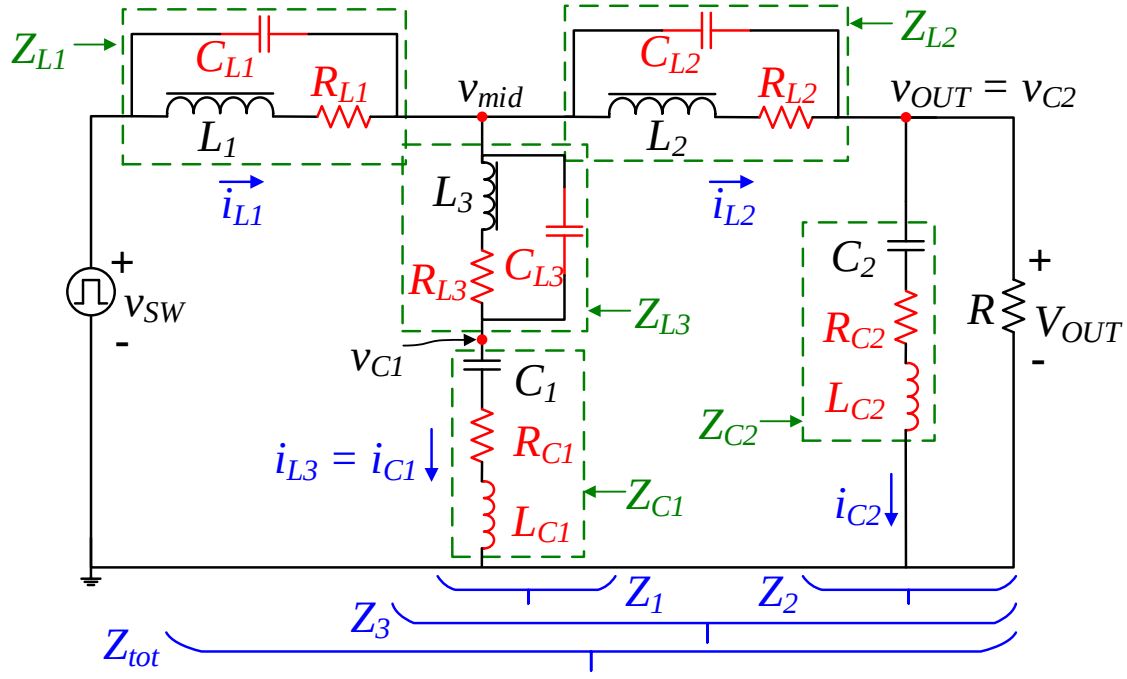


Fig. 5.3 4thRes output filter with parasitic elements.

5.3.1 *s-domain analysis*

To simplify the filter analysis, its components are grouped in the s-domain impedances Z_1, Z_2, Z_3 and Z_{tot}, which are:

$$Z_1(s) = Z_{L3}(s) + Z_{C1}(s) \tag{5.24}$$

$$Z_2(s) = \frac{RZ_{C2}(s)}{R + Z_{C2}(s)} \tag{5.25}$$

$$Z_3(s) = \frac{Z_1(s)\big(Z_{L2}(s) + Z_2(s)\big)}{Z_1(s) + \big(Z_{L2}(s) + Z_2(s)\big)} \tag{5.26}$$

$$Z_{tot}(s) = Z_{L1}(s) + Z_3(s) \tag{5.27}$$

Then the filter gain is divided into two stages, G_1 and G_2 for the 1st and 2nd filter stages, respectively, which are combined to get the overall filter gain G_{filter} as follows:

$$G_1(s) = \frac{v_{mid}(s)}{v_{sw}(s)} = \frac{Z_3(s)}{Z_{L1}(s) + Z_3(s)} \tag{5.28}$$

$$G_2(s) = \frac{v_{out}(s)}{v_{mid}(s)} = \frac{Z_2(s)}{Z_{L2}(s) + Z_2(s)} \tag{5.29}$$

$$G_{filter}(s) = \frac{v_{out}(s)}{v_{sw}(s)} = G_1(s)G_2(s) \tag{5.30}$$

Then the voltages v_{mid}, v_{C1} and v_{C2} are calculated.

$$v_{mid}(s) = G_1(s)v_{SW}(s) \tag{5.31}$$

$$v_{C2}(s) = v_{out}(s) = G_{filter}(s)v_{SW}(s) \tag{5.32}$$

$$v_{C1}(s) = v_{mid}(s)\frac{Z_{C1}(s)}{Z_{L3}(s) + Z_{C1}(s)} \tag{5.33}$$

Then inductor currents i_{L1}, i_{L2} and i_{L3} are calculated:

$$i_{L2}(s) = \frac{v_{mid}(s) - v_{C2}(s)}{Z_{L2}(s)} \tag{5.34}$$

$$i_{L3}(s) = i_{C1}(s) = \frac{v_{mid}(s)}{Z_{L3}(s) + Z_{C1}(s)} \tag{5.35}$$

$$i_{L1}(s) = i_{L2}(s) + i_{L3}(s) = \frac{v_{SW}(s) - v_{mid}(s)}{Z_{L1}(s)} \tag{5.36}$$

This s-domain analysis can accurately predict the frequency components of the voltages and currents of each element. Furthermore, it is used to predict the time domain

waveform, which improves the prediction of each component performance and the steady-state output voltage ripple over different loading conditions.

5.3.2 *Time-domain conversion*

Assuming linear characteristics of the filter components, the time-domain calculations are done using the standard amplitude-phase Fourier representation:

$$f(t) = A_0 + \sum_{n=1}^{N} A_n \cos(n\omega t + \varphi_n) \tag{5.37}$$

where A_0 is the average value, A_n and φ_n are the nth harmonic amplitude and phase, respectively, extracted from the s-domain solution in Section 5.3.1. The number of harmonics N is infinity ideally, but N = 50 was found accurate enough for this study, as increasing N increases the computation time. Hence, the switching node voltage is represented as:

$$v_{SW}(t) = V_{Out} + \sum_{n=1}^{N} V_n \cos\big(n\omega(t - 0.5DT_{SW})\big) \tag{5.38}$$

where V_n is the harmonic amplitude, $V_n = \Delta V_n/2$, presented in (5.10), and T_{SW} is the switching period $T_{SW} = 1/F_{SW}$.

Then v_{C1}, v_{C2}, i_{L1}, i_{L2} and i_{L3} are represented (at $s_n = jn\omega_{SW}$) as follows:

$$v_{C1}(t) = V_{OUT} + \sum_{n=1}^{N} \left|\frac{G_1(s_n)Z_{C1}(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)}\right| V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(\frac{G_1(s_n)Z_{C1}(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)}\right)\right) \tag{5.39}$$

$$v_{C2}(t) = V_{OUT} + \sum_{n=1}^{N} \left|G_{filter}(s_n)\right| V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(G_{filter}(s_n)\right)\right) \tag{5.40}$$

$$i_{L2}(t) = I_O + \sum_{n=1}^{N} \left| \frac{G_1(s_n) - G_{filter}(s_n)}{Z_{L2}(s_n)} \right| V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(\frac{G_1(s_n) - G_{filter}(s_n)}{Z_{L2}(s_n)} \right) \right) \tag{5.41}$$

$$i_{L3}(t) = \sum_{n=1}^{N} \left| \frac{G_1(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)} \right| V_n \cos\left(n\omega_{SW}(t - 0.5DT_{SW}) + \angle\left(\frac{G_1(s_n)}{Z_{L3}(s_n) + Z_{C1}(s_n)} \right) \right) \tag{5.42}$$

$$i_{L1}(t) = i_{L2}(t) + i_{L3}(t) \tag{5.43}$$

where I_O is the DC output current.

As equations (5.39) to (5.43) are in the time domain, they are used to calculate maximum, minimum and RMS values for each filter component, which allows the design and selection of the components.

$v_{OUT}(t)$ from equation (5.40) is used to predict ΔV_{OUT} versus loading and hence adjust the filter design if needed.

5.4 *Design study*

The considered converter steady-state specifications for this study are listed in Table 5.1, which are typical of point-of-load converter requirements for an intermediate step-down stage, which then is followed by a second stage with tighter output voltage regulation as in [13][43][71] for IVR application. The basic buck converter 2nd order output filter in Fig. 5.1(a) is taken as a baseline where the inductance and capacitance are calculated based on inductor current ripple (ΔI_L) and capacitor voltage ripple (ΔV_{OUT}), respectively.

$$L_{2nd} = \frac{V_{OUT}(1 - D)}{\Delta I_L F_{SW}} \tag{5.44}$$

$$C_{2nd} = \frac{\Delta I_L}{8 F_{SW} \Delta V_{OUT}} \tag{5.45}$$

For comparison purposes, the total capacitance is fixed for the 2nd and 4th order filters designs ($C_{2nd} = C_1 + C_2$), so that the improvement in magnetics can be seen. C_1 and C_2 are chosen at the maximum V_{IN} (as a worst-case) according to the procedure explained in Section 5.2.1. As a result, ΔI_L for the 2nd order is set to 36.5%.

To compare the inductors' energy, the calculated currents in the 4th order and 4thRes filters are approximated, as almost all the current ripple in L_1 flows through C_1. So, the current ripple in L_2 can be neglected. This is seen in the inductor current waveforms from the converter simulation in Fig. 5.4, which shows that the current in L_2 is almost DC with negligible ripple. Therefore, the total inductor peak energy is calculated as:

$$E_L \approx \frac{1}{2}\left[L_1\left(I_{DC}+\frac{\Delta I_{L_1}}{2}\right)^2 + L_2(I_{DC})^2 + L_3\left(\frac{\Delta I_{L_3}}{2}\right)^2\right] \tag{5.46}$$

where

$$\Delta I_{L_3} \approx \Delta I_{L_1} \approx \frac{V_{OUT}(1-D)}{L_1 F_{SW}} \tag{5.47}$$

Table 5.1 Converter design specifications.

Symbol	Quantity	Value	Unit
F_{SW}	Switching frequency	20	MHz
V_{IN}	Input voltage	2.5 – 6.6	V
V_{OUT}	Output voltage	1.8	V
I_{DC}	Output DC current	3	A
ΔI_L	Output current ripple	1.1 (36.5%)	A
ΔV_{OUT}	Output voltage ripple	90 (5%)	mV

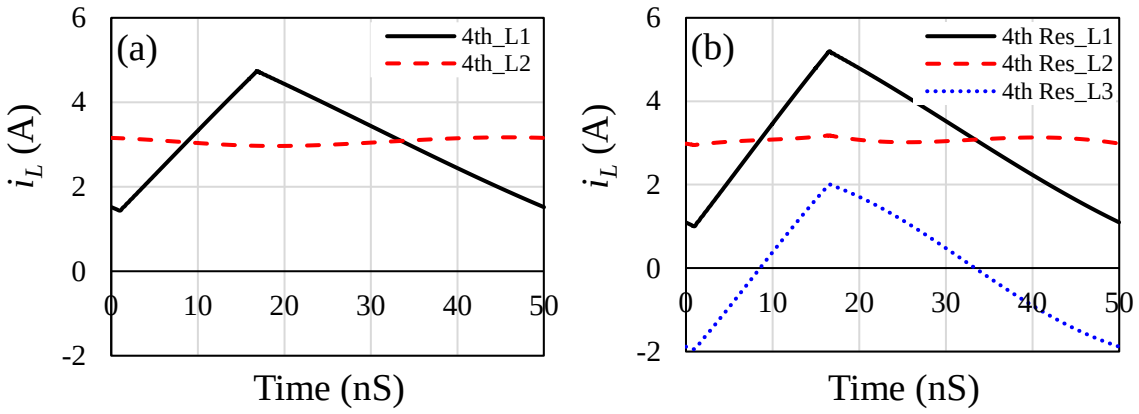


Fig. 5.4 Simulation inductor currents at V_{IN} = 6.6 V: (a) 4th order, (b) 4thRes.

Fig. 5.5 compares the resulting passive component specifications for 2nd order, 4th order and 4thRes filters versus the switching duty cycle. Calculations are based on Butterworth filter parameters. The comparison of the total inductance in Fig. 5.5(a) shows that the 4th order filter required less inductance than the 2nd order filter for duty cycles less than 0.62. Meanwhile, the 4thRes filter achieved smaller inductance than the regular 4th order filter

over almost the whole duty cycle range. It achieved smaller inductance than the 2nd order filter for duty cycles less than 0.74.

The total inductor peak energy in Fig. 5.5(b) reflects a similar relative trend. Moreover, the smallest total inductor peak energy is achieved by the 4thRes filter, which is 35.6% lower than the 2nd order design (at the minimum duty). Note that, practical passive components selection for a converter needs to account for the worst operating condition, i.e. at the minimum duty cycle of 0.27.

The total capacitance comparison in Fig. 5.5(c) shows that the 4thRes filter achieved smaller steady-state capacitance than other configurations. This shows the potential of the 4thRes filter in reducing the size of passive components, with a straightforward design procedure for component selection based on a normalised filter, i.e. a Butterworth filter.

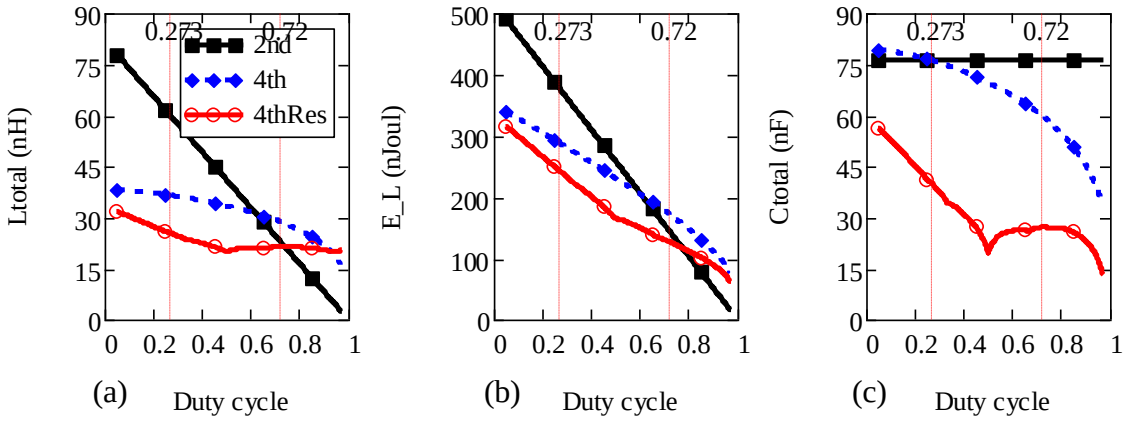


Fig. 5.5 Comparison of passives between 2nd order, 4th order and 4thRes filters at V_{OUT} = 1.8 V, ΔV_{OUT} = 90 mV, I_{DC} = 3 A, F_{SW} = 20 MHz: (a) Total inductance, (b) Total inductors peak energy, (c) Total capacitance.

With the aid of the filter design and analysis in Section 5.2, the filter components chosen for the worst-case duty cycle are compared in Table 5.2, showing the advantages of the 4thRes filter in reducing the passive components. These calculations assume an ESR value of 5 mΩ for C_1 and C_2 branches to account for the parasitic effect in increasing the output voltage ripple in the real converter.

Table 5.2 Design comparison at maximum V_{IN}

Quantity	2nd	4th	4thRes
L1 (nH)	59.7	23.4	15.6
L2 (nH)	-	16.6	8.0
L3 (nH)	-	-	2.06
Total inductance (nH)	59.7	40	25.7

Quantity	2nd	4th	4thRes
Total inductors peak energy (nJoul)	375.8	313	244.5
C1 (nF)	76.2	67	30.8
C2 (nF)	-	16.3	9.6
Total capacitance (nF)	76.2	83.3	40.4
Total capacitors peak energy (nJoul)	129.6	152.2	90

The commercial capacitors selected from Murata for the initial design are shown in Table 5.3. ESR (at 20 MHz) and ESL values were deduced from the datasheet. The 4thRes filter relies on a resonance branch (L_3-C_1), and C_1 consists of four parallel capacitors, each with an effective capacitance of 9.86 nF and parasitic inductance of 0.238 nH. So, the value of L_3 needs to be corrected to 1.55 nH instead of 2.06 nH to maintain resonance at the switching frequency.

Table 5.3 Selected commercial capacitors.

Filter	Cap	PN	C (nF)	ESR (mΩ)	ESL (nH)
2nd	C1	3x GRM2165C1H273JA01	3x 26.8	9.55 /3	0.3 /3
4th	C1	3x GRM2165C1H273JA01	3x 26.8	9.55 /3	0.3 /3
	C2	2x GCM033R71A103KA03	2x 9.68	60 /2	0.21 /2
4th res	C1	4x GRM1555C1E103JE01	4x 9.86	10.4 /4	0.238 /4
	C2	GRM1857U1A103JA44	10.3	18	0.31

The calculated filter gain in (5.30) is shown in Fig. 5.6 for the 4th and 4thRes filters, respectively, (considering parasitic elements) at 0.1 and 3 A load. Fig. 5.6(b) shows the resonance notch at the switching frequency of 20 MHz which attenuates the 1st harmonic significantly, hence allowing for output filter reduction. Furthermore, the predicted time-domain waveforms and ΔV_{OUT} performance of the 4th and 4thRes filters are shown in Fig. 5.7 and Fig. 5.8, respectively, at the maximum V_{IN} of 6.6 V. Attenuation at the resonant frequency can also be seen by comparing v_{C2} and i_{L2} waveforms in Fig. 5.7 and Fig. 5.8, where the ripple frequency in the 4thRes is dominated by the 2nd harmonic at 40 MHz rather than at 20 MHz.

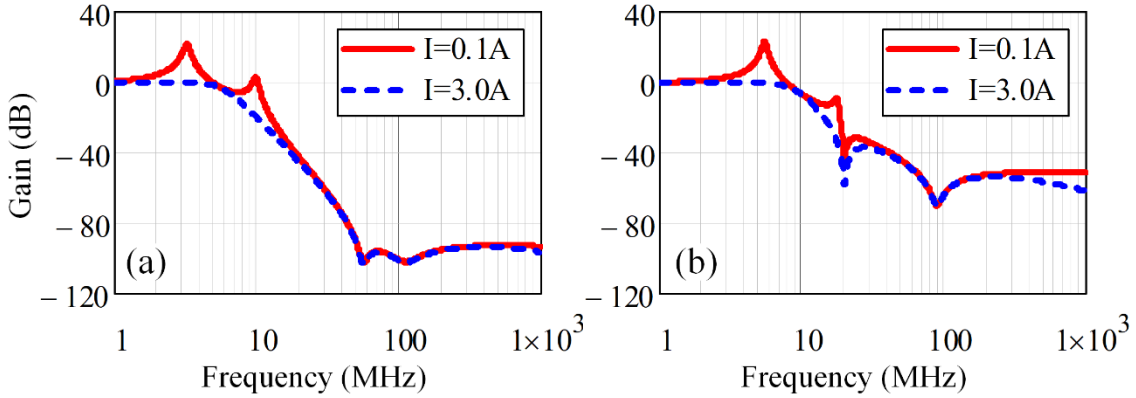


Fig. 5.6 Calculated filter gain at I_{DC} = 0.1 & 3 A: (a) 4th order filter, (b) 4thRes.

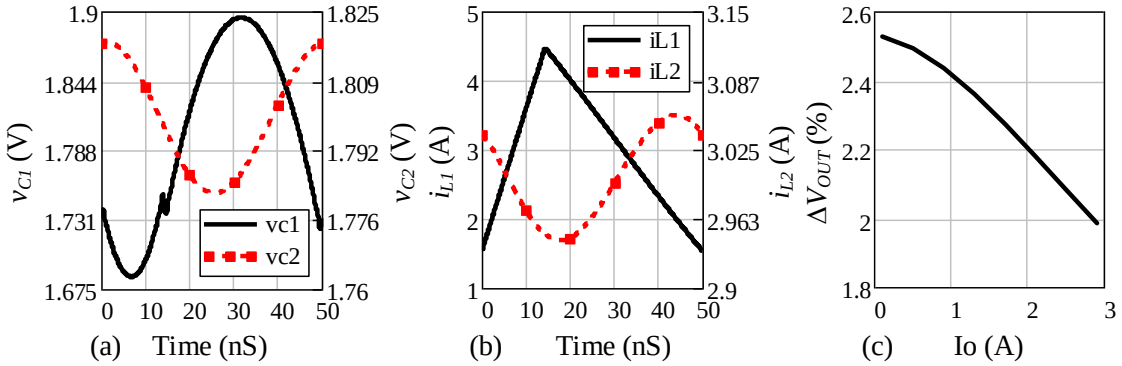


Fig. 5.7 Predicted steady-state performance of the 4th order filter at V_{IN} = 6.6 V, V_{OUT} = 1.8 V, I_{DC} = 3 A, F_{SW} = 20 MHz: (a) $v_{C1}(t)$ and $v_{C2}(t)$, (b) $i_{L1}(t)$ and $i_{L2}(t)$, (c) ΔV_{OUT} vs load.

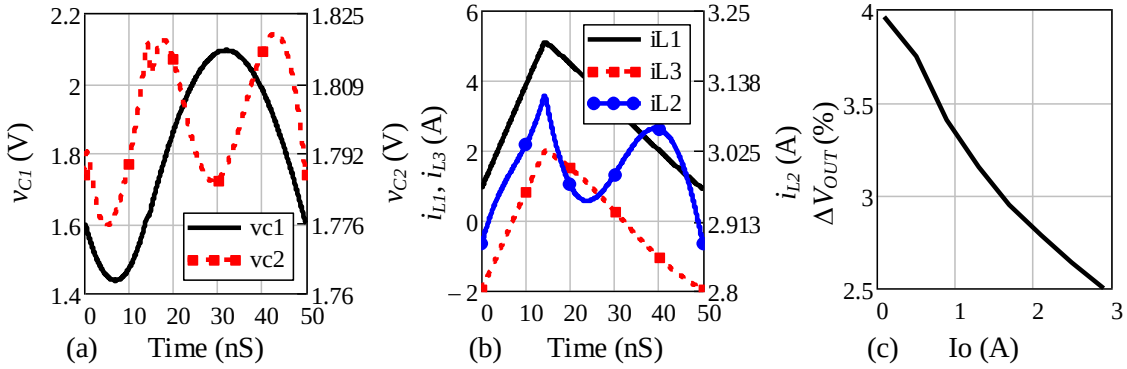


Fig. 5.8 Predicted steady-state performance of the 4thRes filter at V_{IN} = 6.6 V, V_{OUT} = 1.8 V, I_{DC} = 3 A, F_{SW} = 20 MHz: (a) $v_{C1}(t)$ and $v_{C2}(t)$, (b) $i_{L1}(t)$, $i_{L2}(t)$ and $i_{L3}(t)$, (c) ΔV_{OUT} vs load.

Practically, the choice of C_2 is dominated by specifications for voltage over/undershoot during transient load changes rather than steady-state ripple voltage. This may result in a much larger capacitance value for C2, as demonstrated in Section 5.6. However, the procedure outlined here ensures that steady-state specifications are met at least, and any additional transient capacitance would act to reduce the steady-state ripple further.

5.5 *PCB inductor design*

For the prototype converter design, air-core solenoid designs integrated into a standard 2-layer FR4 PCB are considered to illustrate the relative advantage provided by the circuit topologies for inductors fabricated under the same processing constraints. Therefore, while the inductors are not competitive area-wise with inductors having magnetic cores, they illustrate the potential for relative improvement provided by the 4th order topologies. The inductor design is based on PCB manufacturing constraints, i.e. the copper thickness is 70 µm, PCB height is 1.6 mm, via diameter is 0.2 mm, minimum copper trace width and spacing is 0.15 mm, the via annular ring is 0.125 mm, and the minimum solder mask width is 0.07 mm. For this study, the conductor widths are calculated based on the standard IPC-2221A [87] for a temperature rise of 50^{O}C for the maximum inductor RMS current considering passive cooling. The newer standard IPC-2152 [88] can be considered in future work. With these assumptions and constraints, the minimum via-to-via centre spacing is 0.52 mm hence the minimum conductor width is 0.37 mm. The inductance of a PCB solenoid inductor is calculated approximately as:

$$L_S = \frac{\mu_0 {N_T}^2 (W_{Sol} - 2D_{Via})(H_{Sol} - 2T_C)}{(N_T + 1)W_C + N_T S_C} \tag{5.48}$$

where D_{Via} is the PCB via diameter, W_{Sol} & H_{Sol} are the inductor's overall width and height, W_C and T_C are the conductor width and thickness, respectively, and S_C is the conductors spacing.

DC resistance of the solenoid inductor is calculated as:

$$R_{DC} = (N_T + 1)R_{DC\_st} + N_T\left(R_{DC\_dia} + 2R_{DC\_via}\right) \tag{5.49}$$

where R_{DC_st}, R_{DC_dia} and R_{DC_via} are DC resistances of top layer straight conductors, bottom layer diagonal conductors, and PCB via, respectively. R_{DC_via} accounts for a via plating thickness of 25 µm.

Photos of the manufactured inductors are presented in Fig. 5.9, which also shows land footprints for the capacitors listed in Table 5.3. A solenoid design is considered for all inductors except L_3. Its inductance is 1.55 nH which is too small for a solenoid configuration in PCB, so it is achieved by a single strip conductor shown in Fig. 5.9(c).

The inductor sizes are compared in Table 5.4, showing the potential of the 4thRes filter in reducing total inductor size while adhering to practical manufacturing constraints. Size

reduction of the 4thRes filter versus the 2nd order (48%) correlates to some extent with the percentage reduction in the calculated peak energy in Table 5.2 (35%), while there is a similar correlation with the standard 4th order filter (20%) reduction in size versus 17% reduction in peak energy). Differences are due to practical restrictions within a given manufacturing technology. The inductor AC resistance is calculated according to Dowell's analysis [122], similar to [123], $R_{AC,n} = F_n R_{DC}$, where F_n is the resistance factor at the n harmonic. Only the switching frequency component (1st harmonic) is considered for R_{AC} calculation in this study. Then the inductor power loss is calculated as follows:

$$P_{Loss} = \sum_{L_1,L_2,L_3} I_{DC}^2 R_{DC} + \sum_{L_1,L_2,L_3} I_{RMS\_AC}^2 R_{AC} \tag{5.50}$$

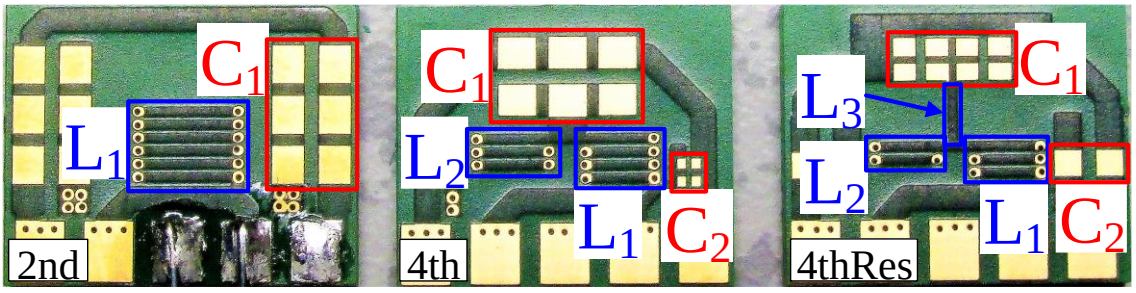
The calculated inductor losses of the three output filters are presented in Fig. 5.10 for the converter specifications listed in Table 5.1. It shows a reduction in full load loss at the cost of light load loss. The AC loss in the 4thRes filter occurs mainly in L_1 (although L_1 and L_3 carry almost the same current ripple) because L_1 is bigger than L_3; hence has a much higher AC resistance of 72.8 vs 7.7 mΩ, as shown in Table 5.4. Overall, there is a trade-off between inductor size and light-load losses, while both size and full load losses are improved for the 4thRes. The inductors' L_S and R_S were measured using an impedance analyser at 20 MHz and shown in Table 5.4, which correlates with the design.

With all output filter components chosen, the overall size of the components is compared in Fig. 5.11, which correlates to some extent with the calculated peak energy in Table 5.2.

Table 5.4 Designed Inductors comparison

	Filter	**2nd**	**4th**		**4thRes**		
Design parameters	Inductor	L_1	L_1	L_2	L_1	L_2	L_3
	L (nH)	59.7	23.4	16.6	15.6	8	1.55
	No. of turns	5	3	2	2	1	0
	Length (mm)	2.98	1.94	1.42	1.42	0.89	2.46
	Width (mm)	4.30	2.98	3.15	2.93	2.77	0.37
	Height (mm)	1.6	1.6	1.6	1.6	1.6	0.07
	Total area (mm^2)	12.8	10.2		7.5		
	Total size (mm^3)	20.5	16.4		10.6		
	R_{DC} (mΩ)	45.6	22.4	16.1	15.4	8.3	1.63

	Filter	2nd	4th		4thRes		
	R_{AC} (mΩ)	216.4	106.1	76.3	72.8	39.2	7.7
FEA at 1 Hz	L_S (nH)	59.90	24.07	16.98	15.81	8.20	1.62
	R_S (mΩ)	45.64	22.53	16.54	15.76	8.89	1.64
FEA at 20 MHz	L_S (nH)	58.3	23.5	16.4	15.3	8	1.55
	R_S (mΩ)	72.6	32.5	26.4	25.2	13.6	4.6
Meas. at 20 MHz	L_S (nH)	58.9	21	18.1	13.88	8.78	1.62
	R_S (mΩ)	230.9	100	77.5	69.21	42.21	7.79



(a) (b) (c)

Fig. 5.9 Manufactured PCB inductors (a) 2nd order, (b) 4th order, (c) 4thRes.

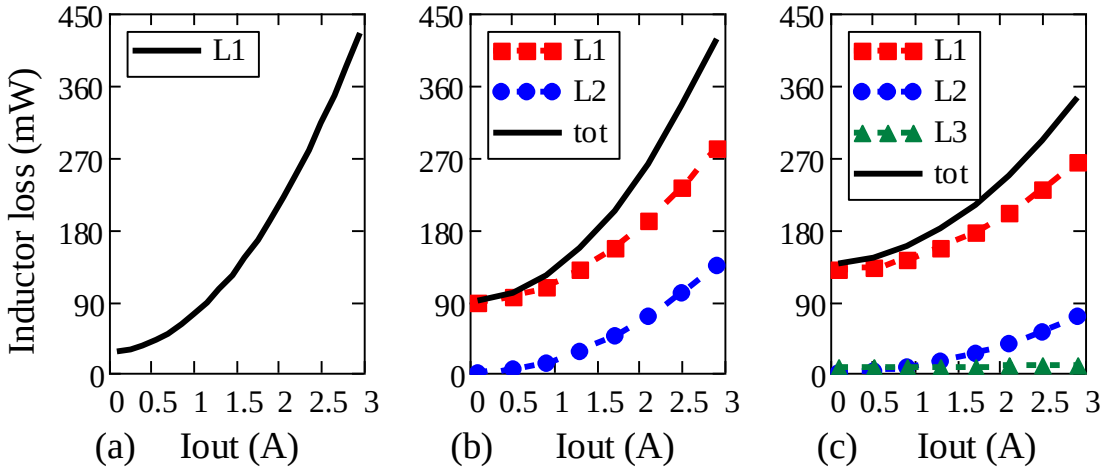


Fig. 5.10 Calculated inductor loss vs load at V_{IN} = 4.5 V: (a) 2nd order, (b) 4th order, (c) 4thRes.

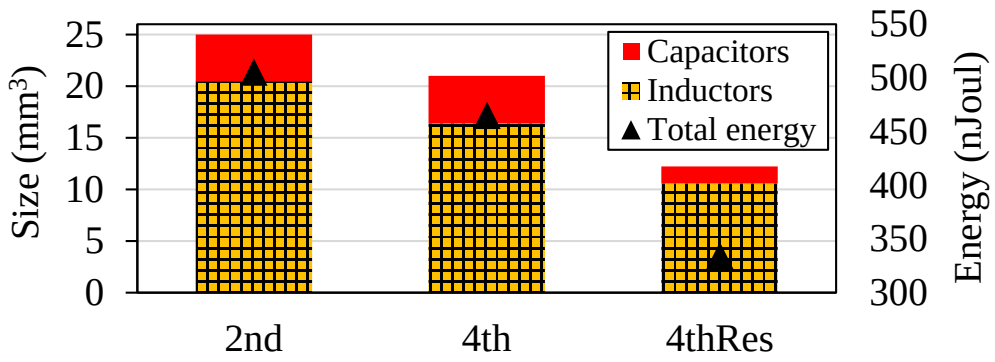


Fig. 5.11 Comparison of the total filter size and predicted total peak energy.

5.6 *Prototype converter performance*

The performance of the converter is investigated in this section with the PCB inductors of Section 5.5, and a buck converter switching stage based on EPC2040 GaN FETs [93] for the high and low sides. The EPC2040 rating is 15 V and 3.4 A, and it has a 745 pC total gate charge, which makes it a suitable device for 20 MHz operation. The switches are driven by the Peregrine PE29102 gate driver, capable of 40 MHz [95]. The Pulse Width Modulation (PWM) input signal is generated using the DIGILENT Nexys3 FPGA development board, i.e. Xilinx Spartan-6 LX16 FPGA chip, and the output is fed into a high-frequency DC/DC converter test motherboard which includes variable resistors for dead-time tuning and output transient capacitors. The FPGA was programmed to generate a 20 MHz signal with the duty cycle adjusted externally. The prototype converter board and the test setup are shown in Fig. 5.12 and Fig. 5.13.

Table 5.5 On-board output capacitors

PN	C (µF)	ESR (mΩ)	ESL (nH)	SRF (MHz)
2x GRM188R61E106KA73	10	20	0.35	2.27
1x GCJ188R71E104KA12	0.1	60	0.3	21.3
4x GCM188R71C105KA49	1	30	0.37	8.7

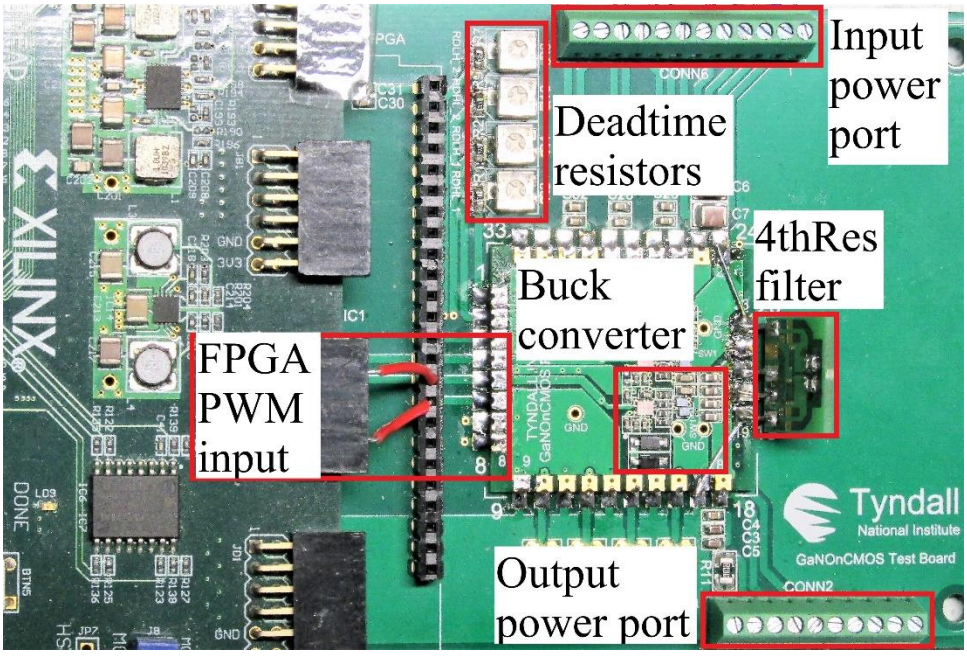


Fig. 5.12 Picture of the prototype converter connected to a test motherboard.

Details of the output capacitor impedances are given in Table 5.5 where parasitic ESR and ESL values were deduced from the datasheet. These values were chosen to enable testing of a range of multi-MHz DC/DC converters under steady-state and transient

conditions. Clearly, they are much larger than values chosen to satisfy steady-state ripple voltage in Section 5.4. However, as is typical in multi-MHz converters, the self-resonant frequency of the larger capacitors selected to satisfy transient conditions may be lower than the switching frequency. Therefore, the smaller capacitors' contribution would be most significant at steady state. The operation of the prototype converter was verified, as shown in the testing waveforms in Fig. 5.14 with the 4thRes filter.

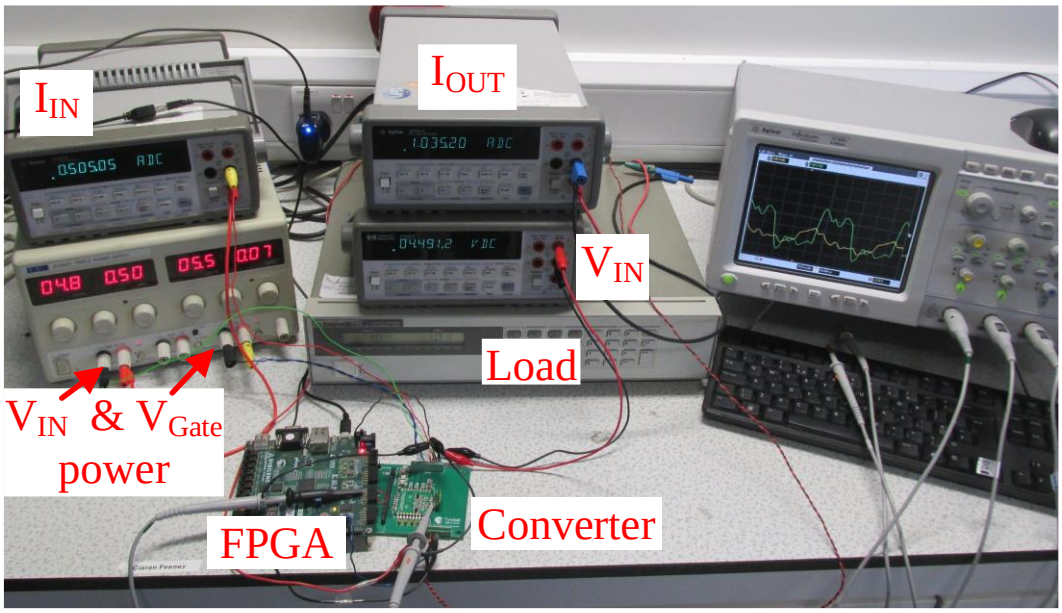


Fig. 5.13 Picture of the test bench setup.

Fig. 5.14 Experimental waveforms with the 4thRes filter at V_{IN} = 4.5 V, V_{OUT} = 1.8 V, I_{OUT} = 2 A and F_{SW} = 20 MHz with 9-bit digital filter enabled, showing the high and low side FETs gate voltage (Vg_HS, Vg_LS), and switching node voltage (Vsw).

5.6.1 *Steady-state performance*

5.6.1.A Output voltage ripple

The measured V_{OUT} waveform is shown in Fig. 5.15 at the nominal V_{IN} of 4.5 V, F_{SW} = 20 MHz and 2 A load. It was measured with only one oscilloscope probe attached to the board to reduce the probes' capacitance effect on the measurement accuracy. Fig. 5.15 shows that ΔV_{OUT} value is much lower than the initial specification of 90 mV for the three filters because the fixed output capacitors (in Table 5.5) are much bigger in value than those chosen in Section 5.4. The measured ΔV_{OUT} value is the same with the 2nd and 4th order filters (9.5 mV), and it is slightly smaller with the 4thRes filter (7.9 mV).

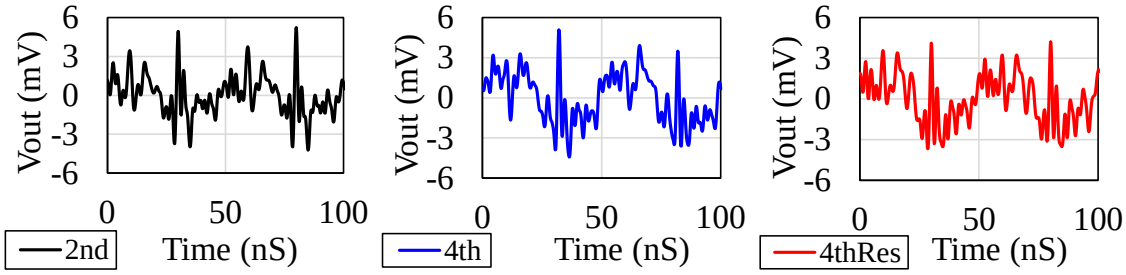


Fig. 5.15 Experimental waveforms of the output voltage (AC coupled) at V_{IN} = 4.5 V, V_{OUT} ≈ 1.8 V, I_{OUT} = 2 A and F_{SW} = 20 MHz.

5.6.1.B Converter efficiency

Open-loop circuit simulation is carried out using LTspice with spice models of EPC2040 switches for the high and low sides and for the output capacitors of Table 5.5. To account for parasitic packaging effects, the simulation model considers inductance and resistance values of 400 pH and 0.2 mΩ, respectively at each FET terminal. The gate signal dead time is 1.1 ns resulting in low-to-high and high-to-low dead-times of ~36 & 123 ps, respectively, between the FETs reaching the switching point voltage, i.e. 2.2 V approximately according to the datasheet [93]. The experimental dead-time was tuned to minimise the overshoot and undershoot in the switching voltage. Simulated and measured converter efficiencies vs output power at the nominal V_{IN} of 4.5 V are shown in Fig. 5.16(a) and (b), respectively. Fig. 5.16(b) includes a curve fit of the measurement data, similar to the method in [124]. The trends in measured efficiency correlate to a large extent with simulation results. Fig. 5.16(b) shows that the 4thRes filter has slightly lower efficiency than the 4th order filter below ~2.5 W. However, the fitted curves show that the full load (5.4 W) measured efficiency of the 4thRes filter is 3.6% and 3.7% higher than the 4th and 2nd order filters, respectively. Overall, the difference between measured and modelled absolute efficiency is likely because of factors not included in the model,

such as PCB packaging interconnect impedances and eddy current effects due to proximity with air-core inductors operating at 20 MHz.

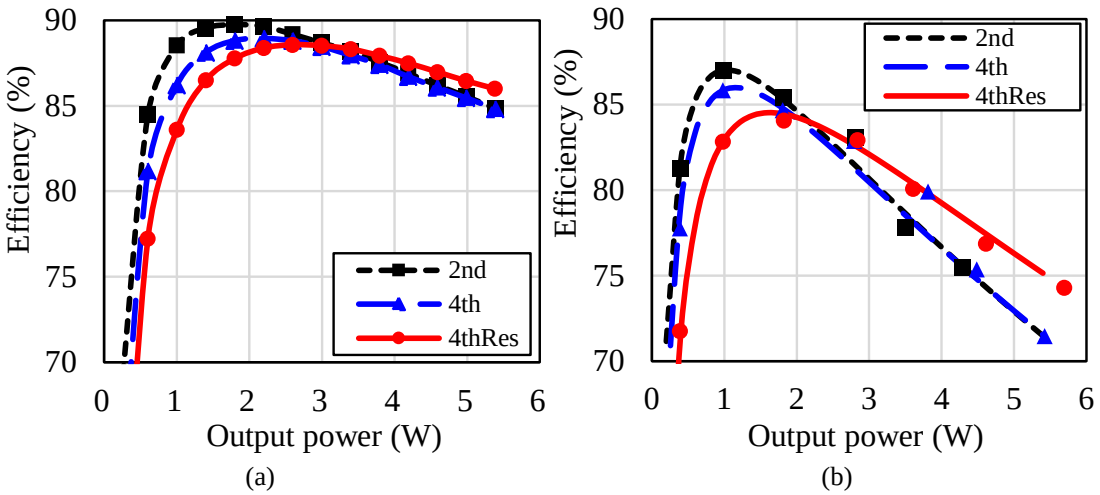


Fig. 5.16 Converter efficiency vs load at V_{IN} = 4.5 V, V_{OUT} = 1.8 V and F_{SW} = 20 MHz: (a) Spice simulation, (b) Measured data and its curve fitting.

5.6.2 *Converter loss breakdown*

The spice simulation loss breakdown at full load of 5.4 W and nominal V_{IN} of 4.5 V in Fig. 5.17 shows that the reduction in total loss of the 4thRes filter is mainly due to the reduction in inductor DC resistance loss and low side FET switching loss.

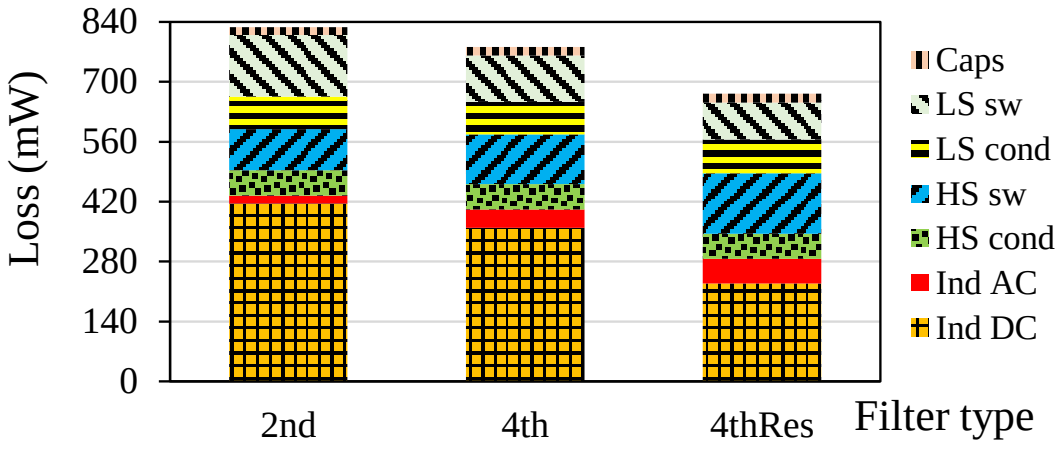


Fig. 5.17 Simulated full load loss breakdown at V_{IN} = 4.5 V.

5.6.3 *Open-loop load transient simulation*

Spice simulation results of V_{OUT} open-loop instant load transition between 10% to 100% load in Fig. 5.18 at V_{IN} = 4.5 V shows that the 4thRes filter has a faster settling time during loading and unloading as an advantage of utilising less overall inductance. Future work will consider closed-loop performance for the 2nd order versus 4thRes filters.

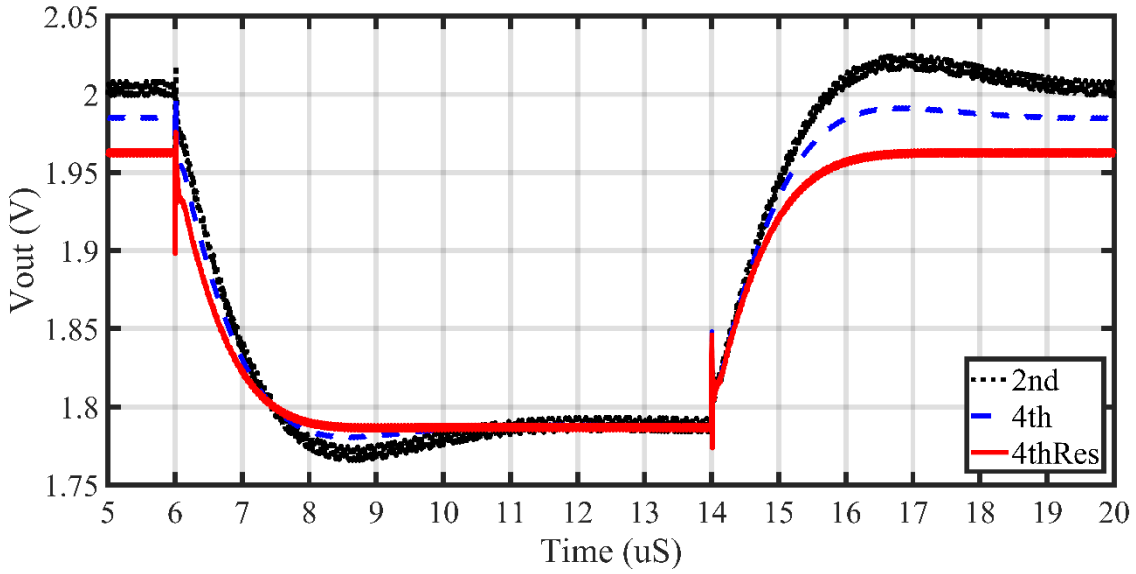


Fig. 5.18 Simulation load transient loading from 10% to 100% at V_{IN} = 4.5 V.

These results show the opportunity and potential of the 4thRes filter as it resulted in a significant reduction in the passive components' size and an increase in the full load efficiency without sacrificing the output ripple, besides having a faster settling time during load transients.

5.7 *Summary*

This chapter presents a novel selection procedure for passive components in a buck converter with Butterworth based 4th order and 4thRes filters. The main motivation is to reduce the size of the output filter, particularly the inductor. Previous studies investigated the resonance effect of the output filter of DC-DC converters provided by coupled inductors; however, a selection method for the filter components in terms of the converter specifications was not provided.

The presented study shows the potential of the 4thRes filter to reduce the size of the passive components over a wide duty cycle range. This is confirmed by PCB solenoid inductor structures based on standard PCB manufacturing process limitations. The outcomes of the design study show the potential of the 4thRes filter compared with a 2nd order filter. For the same output voltage ripple, it provides a 2.4% increase in inductor efficiency at full load, while requiring much smaller passives, i.e., 58% less inductance, 35% less inductor peak energy reflected in 48% less inductor volume. Besides, the 4thRes requires 45% less steady-state capacitance, which results in a 31% reduction in capacitor energy. The prototype converter with the 4thRes filter achieves 3.7% and 3.6% higher full load efficiency than the regular 2nd and 4th order filters, respectively. Moreover, the

4thRes filter simulation shows a faster settling time performance during load transients with the same output capacitance, compared with the 2^{nd} and 4^{th} order filters. These results show that the 4thRes filter can be a suitable replacement for the regular 2^{nd} and 4^{th} order filters in DC-DC converters to achieve smaller passive components, particularly for converters operating at higher load and fixed switching frequency.

Chapter 6 –Topologies Comparison and Discussion

There are many DC-DC conversion topologies; however, not all topologies suit multi-MHz low power converter specifications. Some of the suitable topologies are investigated throughout this thesis, i.e. multiphase buck, multiphase 3-level and 4th order resonance (4thRes) filter topologies in chapters 3, 4 & 5, respectively, along with consideration of coupled inductors. The previous chapters explained and verified the theoretical analysis of these topologies. This chapter presents theoretical comparisons of these topologies in different DC-DC converter applications and a discussion of some trade-offs.

For comparison purposes, a sample of three Point-of-Load (POL) converter specifications are considered specifically for powering (i) a FPGA application as in [125], i.e. considered in previous chapters, (ii) a Single Board Computer (SBC) application similar to the converter in [126], and (iii) an Integrated Voltage Regulator (IVR) in a microprocessor application as in [13]. These are listed in Table 6.1; the specifications are selected close to commercial DC-DC converter products to compare topologies for duty cycles below, around, and above 0.5. The mentioned applications are just samples to extend the theoretical analysis presented in the previous chapters and show its effectiveness for topology selection to minimise the passive components under different circuit conditions. The chosen converter specifications could be found in other applications as well.

Table 6.1 Selected DC-DC converter specifications.

Symbol	Quantity	FPGA	SBC	IVR
F_{SW} (MHz)	Switching frequency	20	20	100
V_{IN} (V)	Input voltage	2.5 – 6.6	5 – 18	1.6 – 2
V_{OUT} (V)	Output voltage	1.8	1.8	1
D	Duty cycle	0.273 – 0.72	0.1 – 0.36	0.5 – 0.625
I_{DC} (A)	Output DC current	3	6	1
ΔI_{Nph} (A)	Output current ripple	0.75 (25%)	1.5 (25%)	0.25 (25%)
ΔI_{Ph_Max} (%)	Maximum phase current ripple	200%	200%	200%
ΔV_{OUT} (mV)	Output voltage ripple	90 (5%)	90 (5%)	10 (1%)
V_{OS} (mV)	V_{OUT} overshoot	90 (5%)	90 (5%)	10 (1%)
I_{Low} to I_{High} (A)	Load transient	0 to 3	0 to 6	0 to 1

The passive components are compared for the FPGA, SBC and IVR converter specifications with the multiphase buck, multiphase 3-level and 4thRes filter topologies in Fig. 6.1, Fig. 6.2 and Fig. 6.3, respectively. This comparison shows how each topology impacts the passive components differently according to the converter specifications. However, there are some common characteristics, e.g., for the multiphase topologies, the inductors' and capacitors' peak energy bottoms out at a minimum level while increasing the number of phases for the three converter specifications because of the applied 200% restriction on the phase current ripple. To compare the proposed analysis vs literature converters, the inductor power density is evaluated by dividing the converter's output power by the inductor peak energy (P_{OUT}/EL_{Pk}), as inductor peak energy represents its size theoretically.

6.1 *Converter for FPGA application*

The converter passive components analysis for FPGA application with wide input voltage range is shown in Fig. 6.1.

In terms of the total inductance and corresponding peak energy shown in Fig. 6.1(a, d), the multiphase 3-level topology performs better than the multiphase buck topology, as the minimum inductor peak energy is achieved by a 2-phase 3-level configuration. This is because 3-Level topology reduces inductor voltage and doubles the frequency, which results in significant reduction in the inductor volt-second stress. However, the novel 4thRes topology design achieves a significant reduction considering the required number of switches, as its inductance is close to a 1-phase 3-level and its inductor energy is close to a 2-phase buck. This reduction is due to filtering out the first harmonic through the resonance branch.

In terms of the total steady-state capacitance and corresponding peak energy shown in Fig. 6.1(b, c), the multiphase buck and 4thRes topologies perform better than the multiphase 3-level topology, as the 3-level requires extra flying capacitor per phase, i.e. load dependant.

In terms of the total load transient capacitance and corresponding peak energy shown in Fig. 6.1(c, f), the multiphase buck topology performs better than the multiphase 3-level topology for the same number of switches, due to the added flying capacitance per phase.

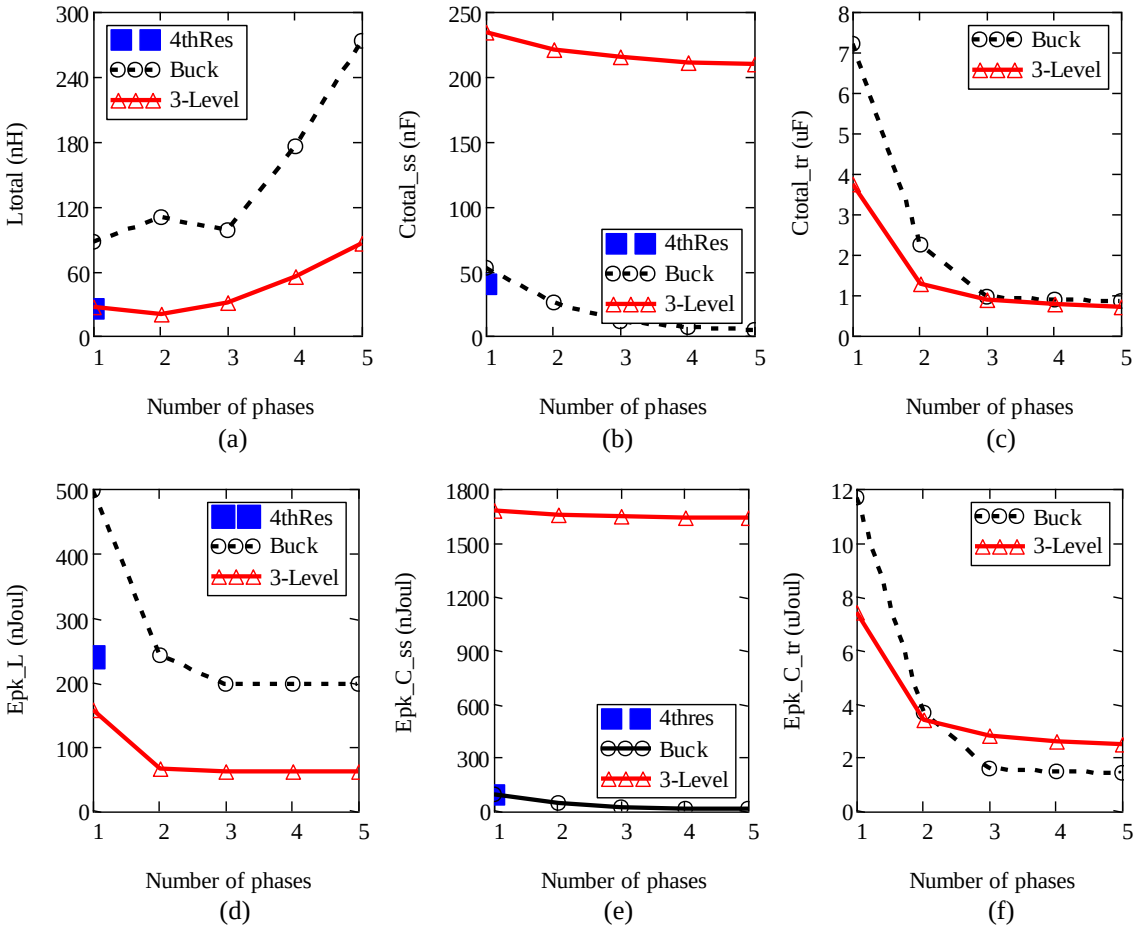


Fig. 6.1 Passive components comparison for mobile FPGA converter specification.

Table 6.2 Comparison sample with literature for FPGA converter specifications.

Symbol	Proposed analysis			[32]	[46]	[63]	[30]
F_{SW} (MHz)	20			10	27	20	47.5
V_{IN} (V)	2.5 – 6.6			3.3	3.3	4.2	2.4-4.4
V_{OUT} (V)	1.8			1.6	1.8	1.8	1-2.2
I_{DC_Max} (A)	3			6	0.4	0.9	0.396
P_{OUT_Max} (W)	5.4			9.6	0.72	1.62	0.87
Topology	Buck	3Level	4thRes	Buck	Buck	Buck	Resonant SC
Nph	3	2	1	4	1	2	2
Ls/phase (nH)	32.8	10.3	25.4	300	60	63.5	3.85
EL_Pk (nJoul)	196.4	64	238.2	1608.6	12.8	46.4	99.2
P_{OUT}/*EL_Pk* (mW/nJoul)	27.5	84.4	22.7	6.0	56.3	34.9	8.8

The proposed analysis of required inductor energy for the FPGA converter specifications is compared with related converters from the literature in Table 6.2. The proposed

analysis optimises the inductor power density (P_{OUT}/EL_{Pk}) over the input voltage range. The literature converters consider input voltage of a single value or a narrow range. The converter in [46] shows very high P_{OUT}/EL_{Pk}; however, it has a lower input voltage (3.3 V) and lower DC current (0.4 A) than this study.

6.2 *Converter for SBC application*

The converter passive components analysis for the SBC application is shown in Fig. 6.2.

The total inductance and corresponding peak energy are shown in Fig. 6.2(a, d). The multiphase 3-level performs better than the multiphase buck topology, almost as in the FPGA application. Interestingly, the novel 4thRes topology analysis achieves significant reduction without increasing the required number of switches, i.e. its inductance is the smallest, and its inductor energy is close to the value achieved by a 1-phase 3-level configuration. The 3-level is not operating at 0.5 duty cycle which can limit its benefits in the inductor energy reduction.

In terms of the total steady-state capacitance and corresponding peak energy shown in Fig. 6.2(b, c), the comparison trends are almost similar to the FPGA application in Fig. 6.1(b, c) respectively, as the multiphase buck and 4thRes topologies perform better than the multiphase 3-level topology.

The total load transient capacitance and corresponding peak energy are shown in Fig. 6.2(c, f). For the same number of switches, the multiphase buck and 3-level topologies perform almost similarly in total capacitance value. However, the multiphase buck performs much better in terms of the total capacitor energy. This significant difference is because the 3-level minimum operating duty cycle (0.1) is far from its best operating point (0.5).

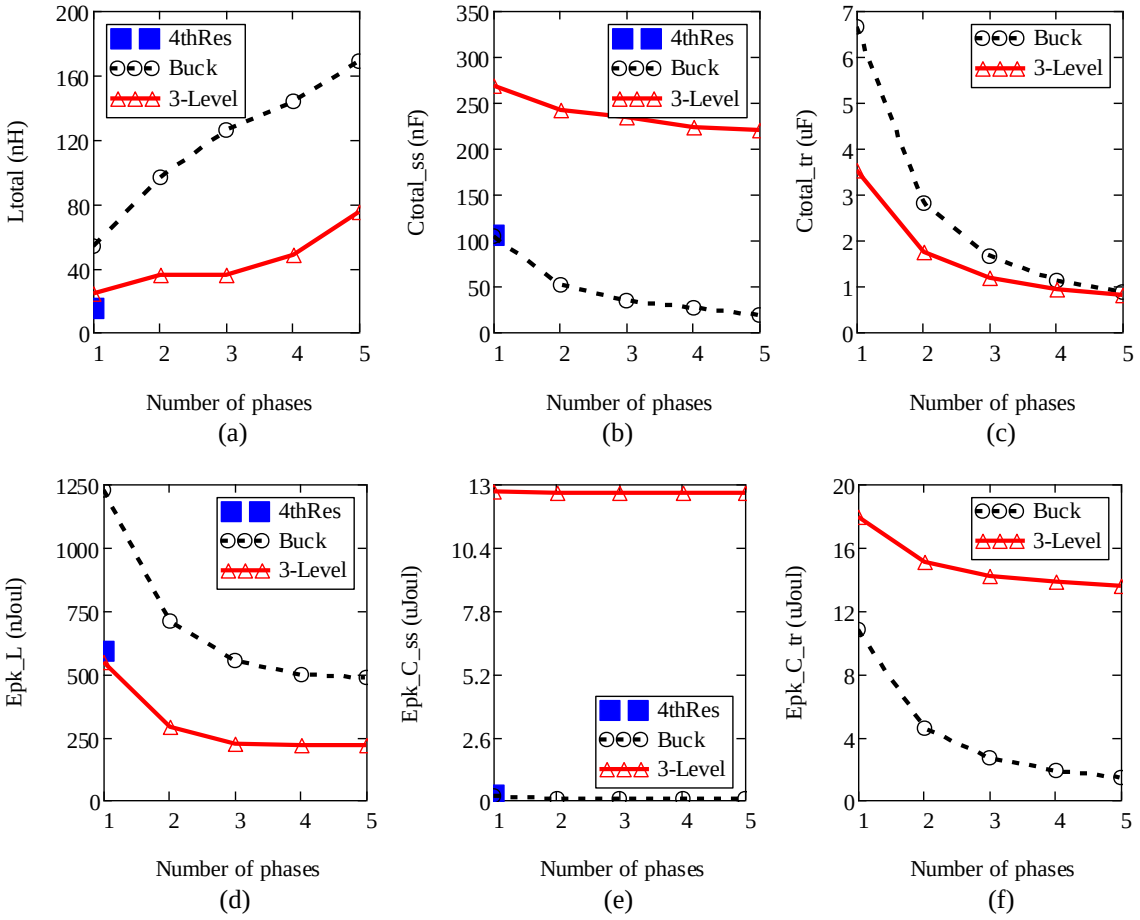


Fig. 6.2 Passive components comparison for SBC converter specification.

Table 6.3 Comparison sample with literature for SBC converter specifications.

Symbol	Proposed analysis			[32]	[50]	[40]
F_{SW} (MHz)	20			10	6	1-5
V_{IN} (V)	5 – 18			3.3	3.6-4	12
V_{OUT} (V)	1.8			1.6	1.2-3	1.8
I_{DC_Max} (A)	6			6	4	5.5
P_{OUT_Max} (W)	10.8			9.6	12	9.9
Topology	Buck	3Level	4thRes	Buck	Buck	Buck
Nph	3	2	1	4	4	1
Ls/phase (nH)	42	18	15.3	300	2320	419.7
EL_Pk (nJoul)	553.6	288	590	1608.6	1457	7217
P_{OUT}/EL_Pk (mW/nJoul)	19.5	37.5	18.3	6.0	8.2	1.4

The proposed analysis of required inductor energy for the SBC converter specifications is compared with related converters from the literature in Table 6.3. The proposed

analysis achieves higher P_{OUT}/EL_{Pk} than the literature converters while considering a significantly wider input voltage range.

6.3 *Converter for IVR application*

The converter passive components analysis is shown in Fig. 6.3 for a higher frequency IVR application with a relatively narrower duty cycle range than the previously mentioned applications.

In terms of the total inductance and corresponding peak energy shown in Fig. 6.3(a, d), the multiphase 3-level performs better than other configurations, as the duty cycle operation range is very close to 0.5, which is the best operating point for the 3-level topology. The 4thRes - compared to the multiphase buck topology - achieves a significant reduction considering the required number of switches, as the increased requirements for more switches and gate drivers could be more than the reduction in the inductor size depending on the semiconductor and inductor devices technology.

In terms of the total steady-state capacitance and corresponding peak energy shown in Fig. 6.3(b, c), the multiphase buck and 4thRes topologies perform better than the multiphase 3-level, however, the 4thRes clearly achieves the smallest values.

The total load transient capacitance and corresponding peak energy are shown in Fig. 6.3(c, f). For the same number of switches, the multiphase buck topology performs better than the multiphase 3-level. However, both topologies get closer to the same capacitance values as the number of phases increases.

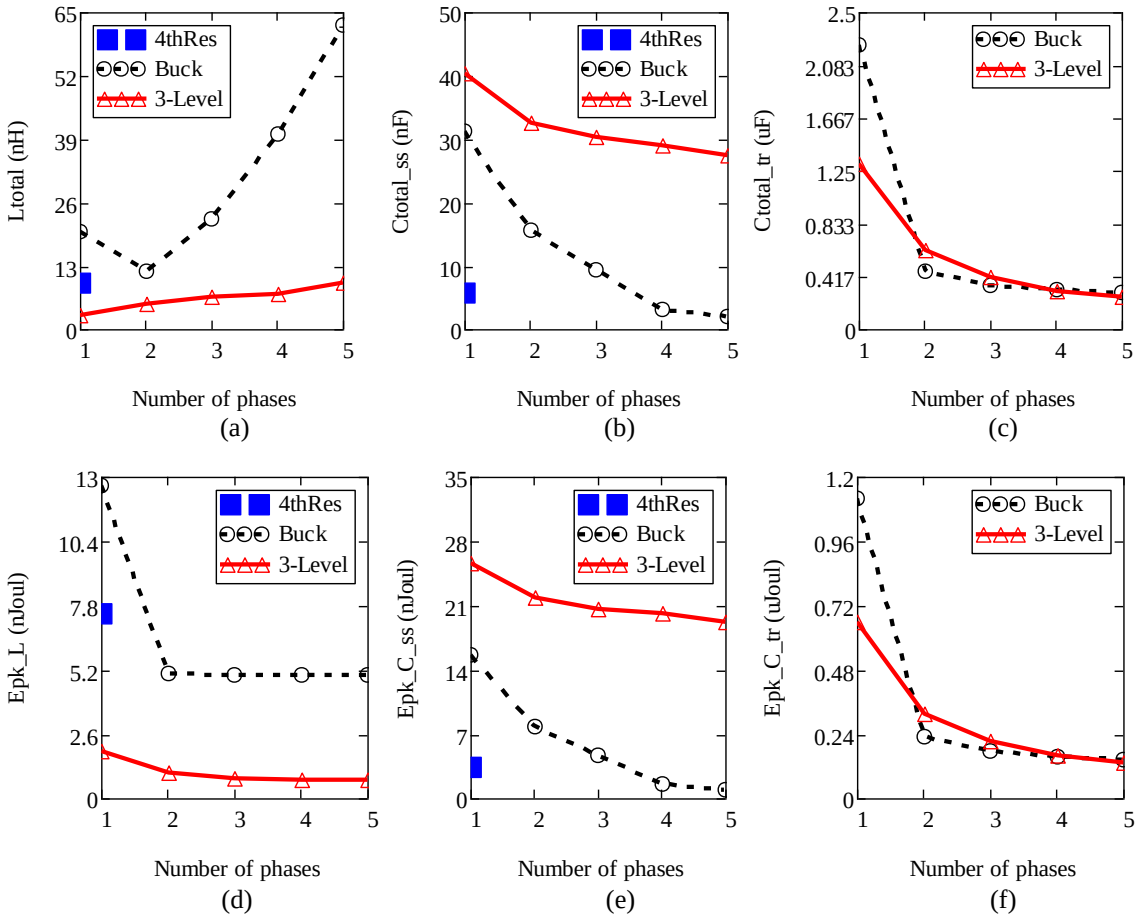


Fig. 6.3 Passive components comparison IVR specification.

Table 6.4 Comparison sample with literature for IVR converter specifications.

Symbol	Proposed analysis			[7]	[58]	[71]	[14]	[75]	[98]
F_{SW} (MHz)	100			0.75-225	20-100	100	40	30-80	200
V_{IN} (V)	1.6 – 2			2-2.6	1.6-2	1.8	1.8	1.8	1.7
V_{OUT} (V)	1			1.1-1.5	0.6-1.2	0.85	0.3-1.6	0.6-1.2	0.9-1.05
I_{DC_Max} (A)	1			0.53	1	20	0.15	1.5	0.8
P_{OUT_Max} (W)	1			0.8	1.2	17	0.24	1.8	0.84
Topology	Buck	3Level	4thRes	Buck	Buck	Buck	3Level	Buck	Buck
Nph	2	2	1	4	2	16	2	8	16
Ls/phase (nH)	5.9	2.6	9.6	3.9	200	8	500	38	2.1
EL_Pk (nJoul)	5.034	1.07	7.5	1.9	52.1	149.9	3.3	9.75	5.16
P_{OUT}/EL_Pk (mW/nJoul)	198.6	934.6	133.3	421.1	23.0	113.4	72.7	184.6	162.8

The proposed analysis of required inductor energy for the IVR converter specifications is compared with related converters from the literature in Table 6.4. The proposed

analysis optimises P_{OUT}/EL_{Pk} over a narrow input voltage range, and the literature converters have a similar range or a single value. The converter in [7] achieves a high P_{OUT}/EL_{Pk}; however, its switching frequency is higher than twice this study.

The three previously presented comparisons can be gathered and summarised from the perspective of the inductor power density vs conversion ratio. As the inductor peak energy is the theoretical representation of the inductor size, the theoretical inductor power density is assumed $= \frac{P_{OUT\_Max}}{EL\_Pk}$. This comparison is shown in Fig. 6.4. In comparison to the literature, the followed procedure allows optimising the theoretical inductor power density, as seen in the trend of the shaded area on the plot. This helps to evaluate the converter topology, regardless of the inductor type.

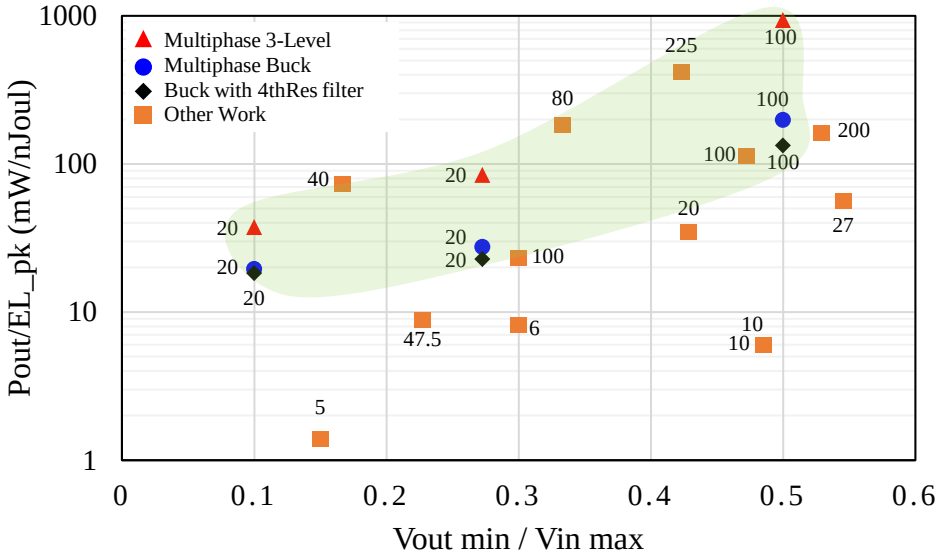


Fig. 6.4 Theoretical inductor power density vs conversion ratio.

6.4 *Summary*

This chapter applied the theoretical analysis presented and verified in chapters 3, 4 & 5 to study the impact of different topologies on the passive components for three DC-DC step-down converter specifications based on commercial applications of the DC-DC converters. The study showed some common behaviour, i.e. passive components peak energy and total load transient capacitance reach minimum values while increasing the number of phases in multiphase buck and multiphase 3-level topologies as a result of restricting the maximum phase current ripple at 200%, meaning that practically considering the addition of switches and driver components limit the advantages of the added phases. Besides, in multiphase topologies, the inductors' overall size does not

reduce linearly with the reduced peak energy, as the manufacturing capabilities are limited to minimum dimensions, which force the inductor size to increase at some point.

Moreover, the proposed analysis of the 4thRes topology showed its capability to reduce the passive components' values and energy without increasing the number of switches, especially for the FPGA and SBC converter specifications.

Similar results on the passive component analysis in multiphase buck and 3-level topologies with 100% phase current ripple maximum limit is presented in Appendix A.

Concluding from investigations throughout this study, the proposed procedure to select the converter topology to optimise magnetics utilisation is summarised in Fig. 6.5. The highlighted boxes are where the thesis's main contributions.

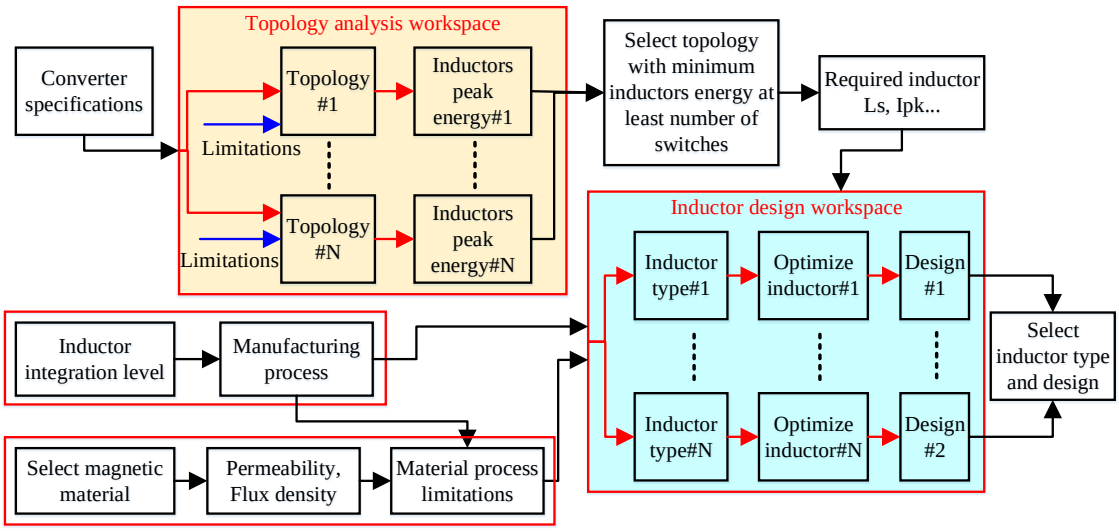


Fig. 6.5 Summary of the proposed converter topology selection to optimize magnetics utilization.

Chapter 7 – Conclusions and Future Work

7.1 *Introduction*

This chapter concludes the study by summarising the key research findings in relation to the research objectives and contributions. It also proposes opportunities for future research.

This thesis addresses the power converter topologies' impact on the size of the passive components, particularly inductors. This helps in topology selection for improved converter power density, especially for low power applications, where the user end device size is a competitive requirement in the market. The thesis proposes a procedure for better utilization of inductors in multiphase buck and 3-level topologies through effective selection of the number of phases, besides presenting a guideline for coupling factor selection of 2-phase coupled inductors in these topologies. It also proposes output filter size reduction in a single-phase buck converter through a novel design procedure of a 4^{th} order resonance filter type.

7.2 *Key findings and contributions*

This thesis contributed to better utilization of passive components, particularly inductors in DC-DC power converters, through analysis of peak energy requirements for given converter specifications.

7.2.1 *Multiphase buck and multiphase 3-level topologies*

For optimum topology selection purposes, this thesis investigated the multiphase buck and 3-level topologies in terms of increasing the number of phases impact on the size of the passive components. It considered wide input voltage converter specifications and restrictions on the current ripple per phase, which was found to limit the reduction of the passive components' peak energy while increasing the number of phases. That means increasing the number of phases is not necessarily beneficial to reducing the passive components' size. The study considered PCB integrated air-core inductors while applying the PCB manufacturing limitations, which showed that after a certain number of phases in a multiphase configuration, the total size of the inductors grows with increasing number of phases. Hence, a multiphase topology that achieves the minimum inductor peak energy with the least number of switches is the ideal choice to optimize overall inductors size. A 20 MHz 5.4 W 2-phase buck converter prototype was

implemented and tested with GaN FET switches and PCB solenoid and spiral inductors to demonstrate the converter operation and efficiency.

7.2.2 *Coupled inductors in multiphase interleaved topologies*

This study presented coupling factor selection guidelines for a 2-phase inversely coupled inductor in a multiphase buck and multiphase 3-level converter topologies for wide input voltage range specification. The main aim of this procedure is to avoid the phase inductance roll-off under all operating conditions within the input voltage range.

7.2.3 *4th order resonance low pass output filter (4thRes)*

A novel straightforward design procedure was presented for the 4th order and 4thRes output filters in a single-phase buck converter based on the normalized Butterworth filter parameters and compared with the 2nd order filter as a baseline. An accurate filter analysis in the s-domain and time-domain was presented to predict the voltages and currents in the filter components. The proposed filter design procedure showed that the 4thRes is capable of reducing the total inductor and capacitor values and size significantly for the same converter specifications and output voltage ripple. A 20 MHz 5.4 W buck converter prototype was implemented and tested with GaN FET switches and PCB solenoid inductors for the 2nd order, 4th order and 4thRes filters. The 4thRes filter significantly improved the full load efficiency because of the reduced inductor resistance at nearly the same output voltage ripple.

7.3 *Future work*

The research work presented in this thesis creates research opportunities in some areas:

- Applying the same analysis to investigate the impact of other topologies on the passive components peak energy, considering each topology's practical limitations to enable a common comparison based on given circuit specifications. This can form an evaluation procedure for the old and new coming converter topologies, which will help in converter topology evaluation to reduce the passive components, increase the converter power density, save energy, and reduce the manufacturing materials consumption.
- Investigating ways to understand the impact of the number of phases in interleaved topologies on the performance and scaling of the switching devices and gate drivers including pull up/down resistors and bootstrap components.

- Develop more inductor design models (e.g. closed core, open core, gapped core, air core) for different structures (e.g. solenoid, spiral, racetrack, stripline, toroid) to optimize the overall Q-factor per volume (or per footprint area), including the manufacturing process design rules. Initial analysis of the results of this study showed that Q-factor per volume is a suitable figure-of-merit for inductor design for DC-DC converters, as detailed in Appendices B and C.
- The 4thRes topology also requires more research in terms of the topology control and dynamics to improve light-load efficiency and predict load transient output voltage overshoot and undershoot.

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Appendix A. Multiphase buck and multiphase 3-Level analysis at phase current ripple maximum limit of 100%

The topologies comparisons were presented in chapter 6 with the phase current ripple limited at 200% in the multiphase topologies, and it is presented here at 100% limit to show the effect of changing the maximum limit of the phase current ripple on the passive components. In general, the noticeable change is that it increased the minimum achievable peak energy of the total inductors and load transient capacitors especially in the multiphase buck topology, which means that the required inductors and capacitors size will increase.

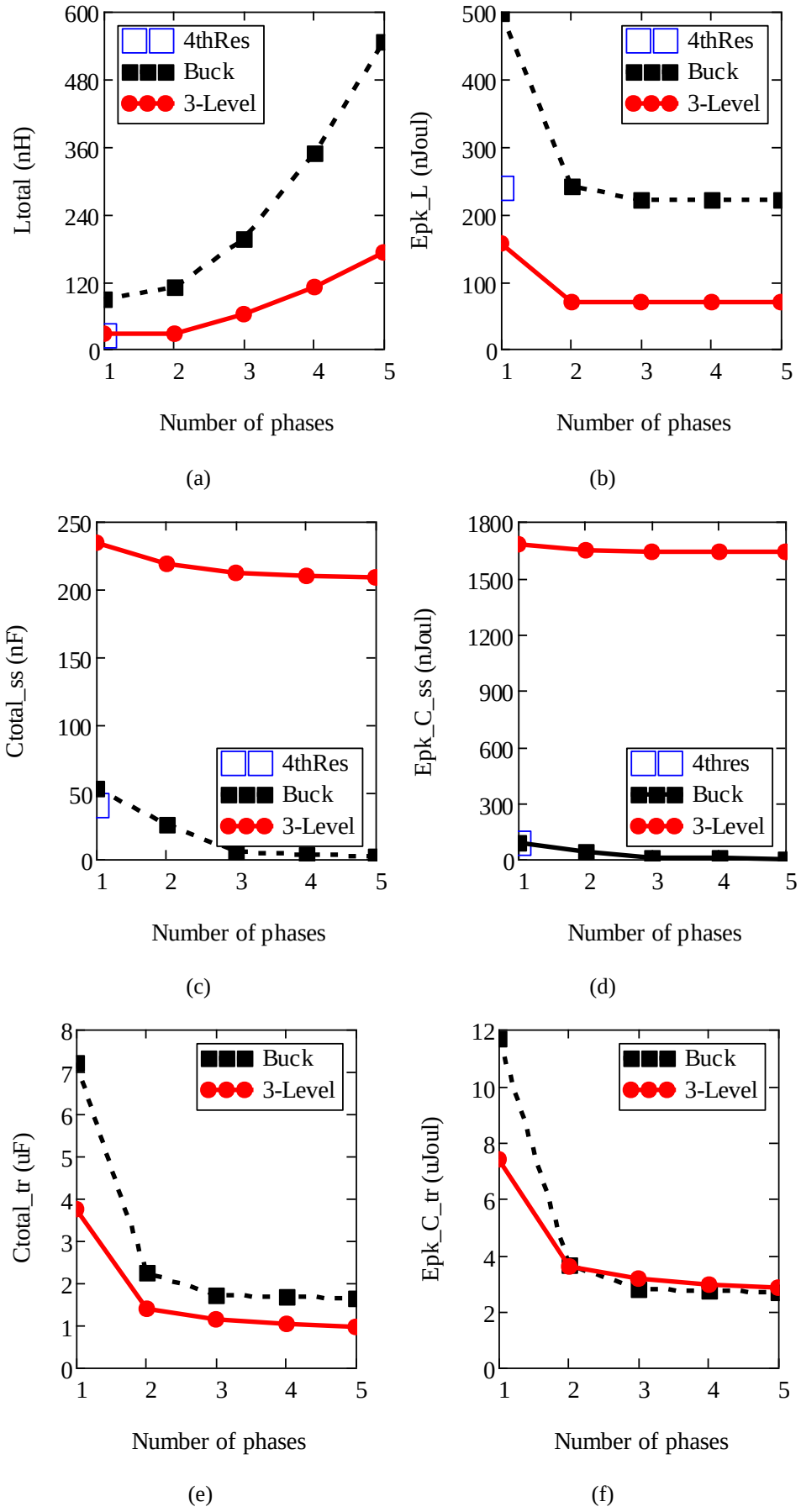

Fig. A.1 Passive components comparison for mobile FPGA converter specification.

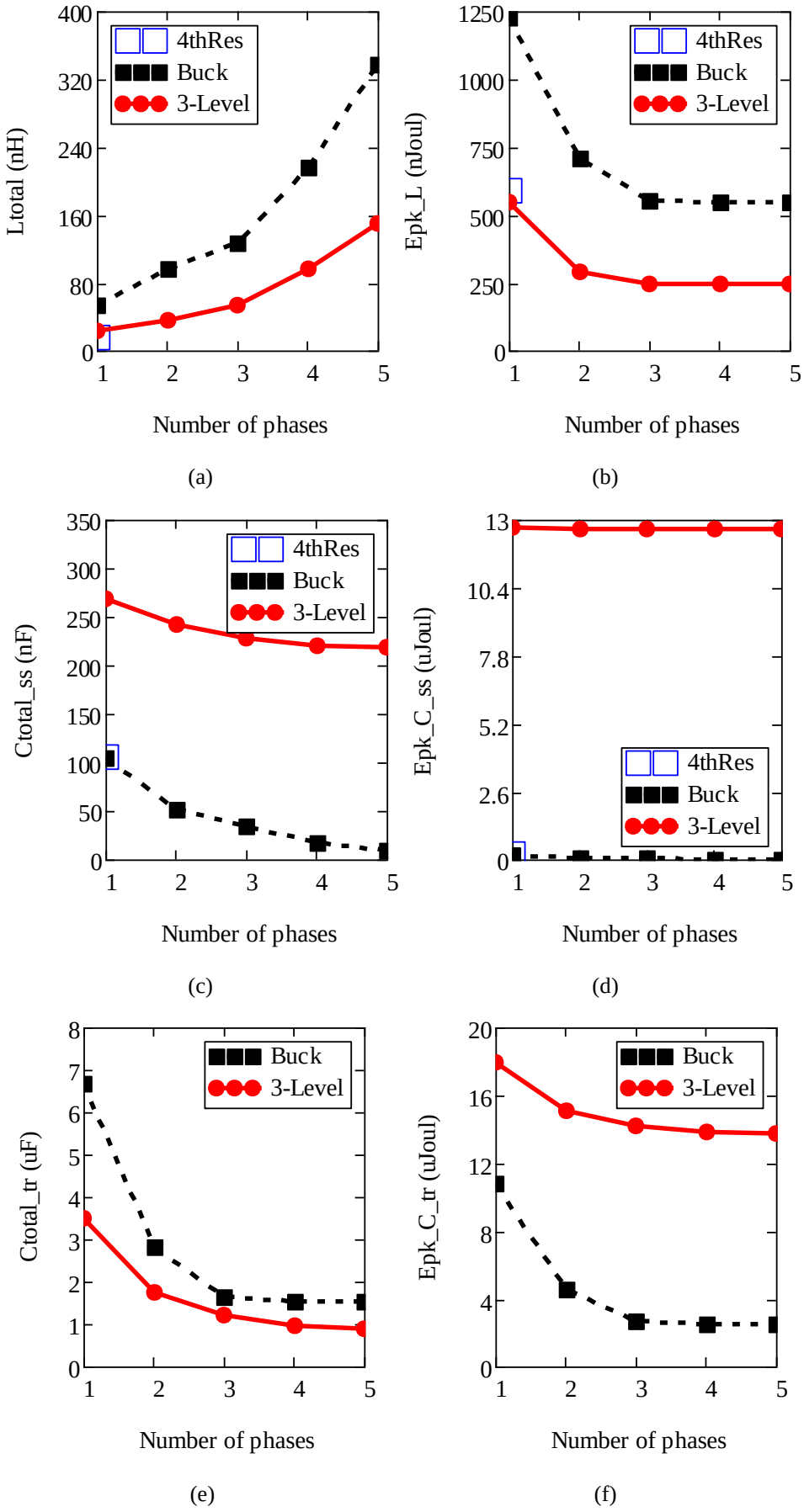

Fig. A.2 Passive components comparison for SBC converter specification.

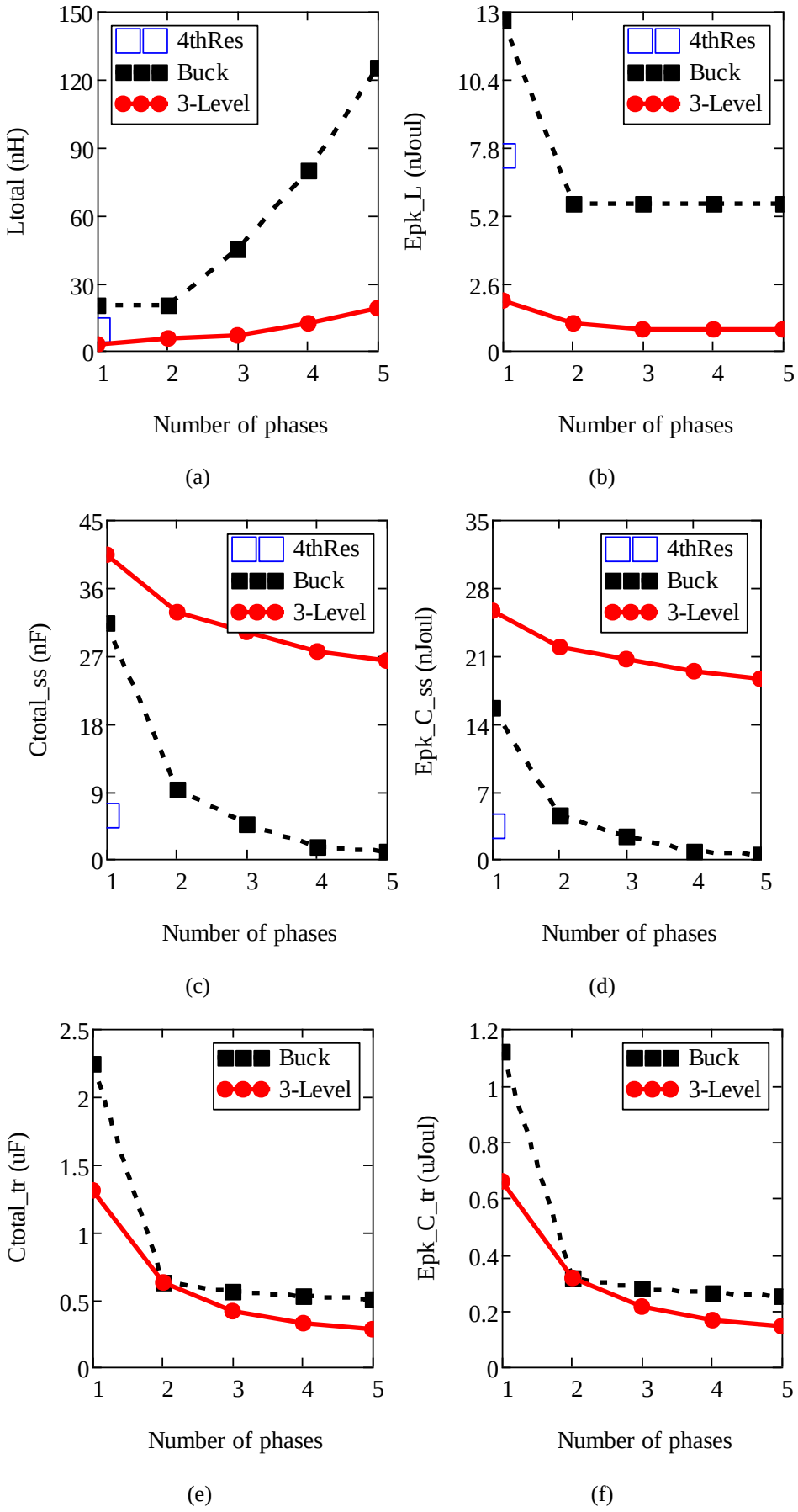

Fig. A.3 Passive components comparison IVR specification.

Appendix B. PCB Solenoid Inductor Design

The basic structure of the PCB solenoid inductor is shown in Fig. B.1 with dimensions designations.

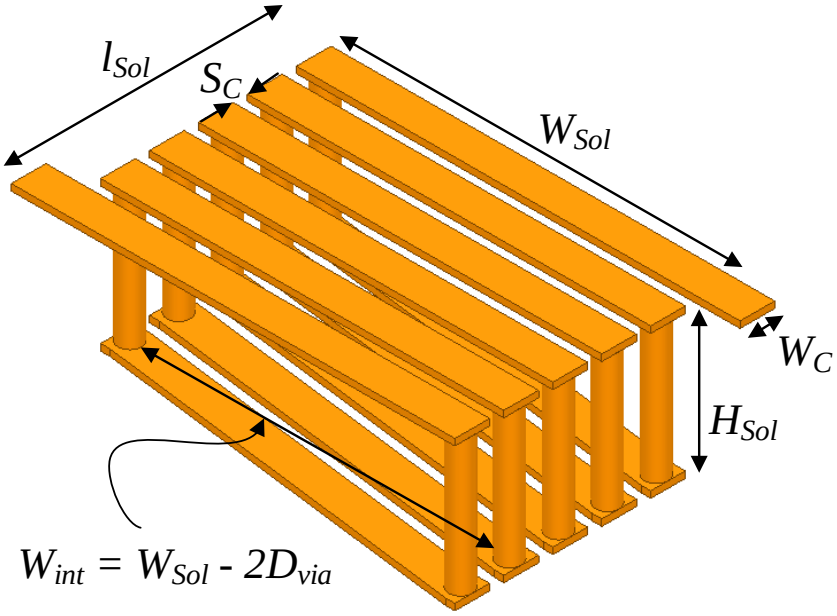

Fig. B.1 PCB solenoid inductor structure.

where W_C is the conductor width, S_C is the conductors spacing, l_{Sol}, W_{Sol} & H_{Sol} are the inductor's overall length, width, and height, respectively, W_{int} is the internal width defined as a via-to-via dimension ($W_{int} = W_{Sol} - 2D_{Via}$).

B.1 Inductance

Based on the solenoid inductance basic equation, the PCB solenoid inductance can be calculated approximately as:

$$L_S = \frac{\mu_0 N_T{}^2 W_{int}(H_{Sol} - 2T_C)}{(N_T + 1)W_C + N_T S_C} \quad \text{(B.1)}$$

where μ_0 is the air permeability $\mu_0 = 4\pi 10^{-7}$, N_T is the number of turns, D_{Via} is the PCB via diameter, and T_C is the conductor thickness.

B.2 PCB manufacturing related parameters

D_{Via}, S_C, T_C and H_{Sol} are predetermined according to the PCB manufacturer capabilities. As D_{Via} is determined according to the available drilling tools diameter e.g., to achieve D_{Via} = 0.2 mm the manufacturer uses a drilling tool with 0.25 mm diameter. S_C should not exceed the minimum values determined by the manufacturer (i.e., typically 0.15 mm) to ensure design manufacturability. T_C is equal to the PCB copper thickness which is selected from dedicated values offered by the manufacturer e.g 35 or 70 µm. H_{Sol} is equal to the PCB height which is selected from dedicated values offered by the manufacturer.

B.3 Conductor width selection

The conductor width W_C is calculated according to the standard IPC-2221A [87] for a temperature rise ΔT of 50 ^{O}C at the RMS full load current as follows with dimensions in mm.

$$W_C = \frac{1}{T_C}\left(\frac{I_{RMS}}{k\Delta T^{0.44}}\right)^{\frac{1}{0.725}} 25.4^2 10^{-6} \tag{B.2}$$

where k is a constant which equals 0.024 or 0.048 for internal or external layers, respectively. Future work can use the newer standard IPC-2152 [88], [89].

B.4 Diagonal conductors spacing

While S_C has a minimum value of 0.15 mm, it may be required to be increased to keep the perpendicular spacing between the diagonal conductors S_{C_dia} on the PCB bottom layer ≥ 0.15 mm, as shown in Fig. B.2. This is necessary to meet the PCB manufacturing capabilities. The difference between S_C and S_{C_dia} values becomes more significant at small inductor width values.

S_C is driven for calculation as follows:

$$S_C = \frac{W_C {S_{C\_dia}}^2 + S_{C\_dia}(W_{int} + D_{via})\sqrt{(W_{int} + D_{via})^2 + {W_C}^2 - {S_{C\_dia}}^2}}{(W_{int} + D_{via})^2 - {S_{C\_dia}}^2} \tag{B.3}$$

This complicates solving (B.1) analytically, but it can be solved using numerical software.

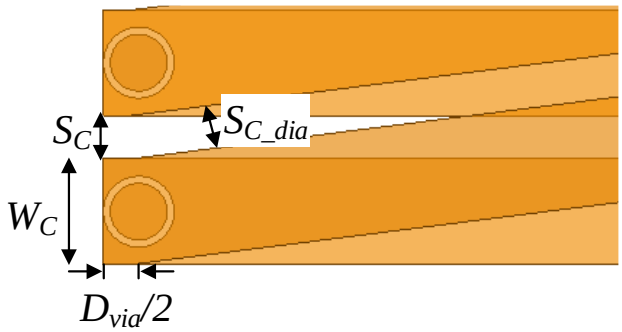

Fig. B.2 Straight conductors spacing and diagonal conductors spacing.

B.5 Internal width and number of turns

With the previously mentioned assumptions for the PCB solenoid inductor, L_S is reduced to a function of (N_T, W_{int}). As N_T is an integer number, a practical range of N_T can be defined (e.g., 1-14 turns) then solve (B.1) numerically for W_{int} at the required L_S value.

B.6 PCB solenoid design example

For inductance requirement of 90 nH at ΔT = 50 ^{O}C and DC current rating of 3A, N_T range is defined 1 to 14 turns, for each N_T value W_{int} is calculated at L_S = 90 nH. For practical PCB layout, the dimensions in mm are rounded up for one decimal place. Then L_S is recalculated to make sure that selected dimensions and number of turns are correct, results for L_S and W_{int} vs N_T is shown in Fig. B.3.

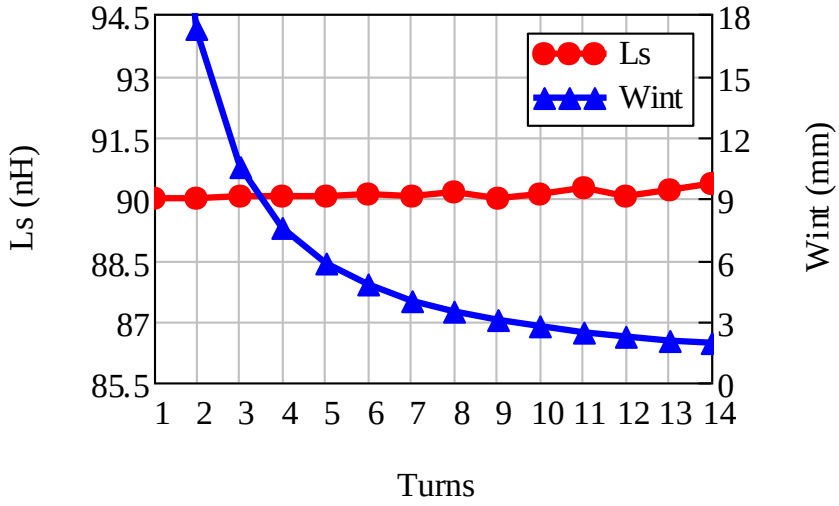

Fig. B.3 Designs of 90 nH inductor.

B.7 DC resistance

DC resistance of the solenoid inductor can be calculated as:

$$R_{DC} = (N_T + 1)R_{DC\_st} + N_T\left(R_{DC\_dia} + 2R_{DC\_via}\right) \quad \text{(B.4)}$$

where R_{DC_st}, R_{DC_dia} and R_{DC_via} are DC resistances of straight conductors, diagonal conductors, and PCB via, respectively, and are calculated as follows:

$$R_{DC\_st} = \frac{\rho(W_{int} + D_{via})}{W_C T_C} \quad \text{(B.5)}$$

$$R_{DC\_dia} = \frac{\rho\sqrt{(W_{int} + D_{via})^2 + (W_C + S_C)^2}}{W_C T_C} \quad \text{(B.6)}$$

$$R_{DC\_via} = \frac{4\rho H_{Sol}}{\pi(D_{via} + 0.05)^2 - \pi {D_{via}}^2} \quad \text{(B.7)}$$

B.8 AC resistance

The inductor AC resistance R_{AC} is a frequency dependant increase in the inductor resistance due to skin effect and proximity effect phenomenon caused by the AC component of the inductor current. The inductor AC resistance is calculated according to Dowell analysis [122], similar to [123], $R_{AC,n} = F_n R_{DC}$, where F_n is the resistance factor at the n harmonic. Only the switching frequency component (1st harmonic) is considered for R_{AC} calculation in this study.

B.9 Inductor power loss

Total inductor power loss is more simplified with air-core inductor than inductor with magnetic core because of the absence of the core loss nonlinearities, and it is calculated as follows:

$$P_{Loss} = I_{RMS\_DC}^2 R_{DC} + \sum_n I_{RMS\_AC}^2 R_{AC} \quad \text{(B.8)}$$

The effect of the number of turns on the calculated inductor loss and volume is shown in Fig. B.4.

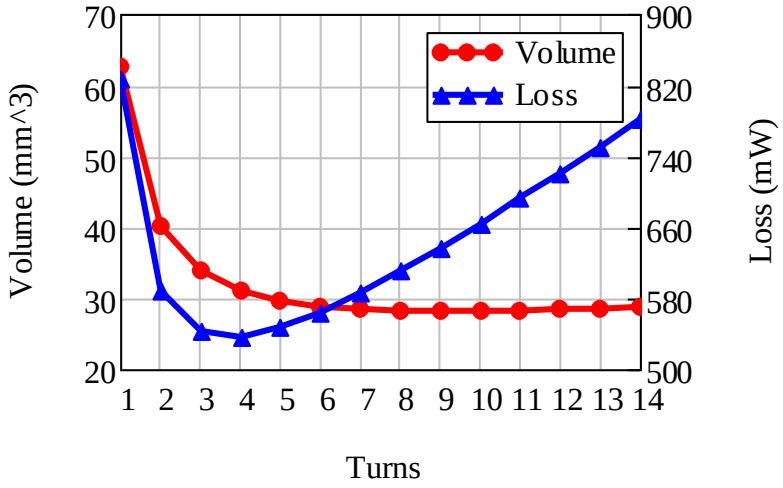

Fig. B.4 Calculated loss and volume of a 90 nH inductor.

B.10 Overall Q-factor

The inductor's overall Q-factor is a performance benchmarking parameter, and it is calculated considering the overall inductor power loss at the switching frequency F_{SW} as:

$$Q_{Overall} = F_{SW}\frac{0.5L_S(I_{DC}+0.5\Delta I)^2}{P_{Loss}} \tag{B.9}$$

For an optimum choice of the number of turns, $Q_{Overall}$ per inductor volume is considered for benchmarking and design point selection where the maximum ($Q_{Overall}$ / *Volume*) value is achieved. The inductor ($Q_{Overall}$ / *Volume*) and loss are presented in Fig. B.5 for the 90 nH inductor example, and it shows that the maximum ($Q_{Overall}$ / *Volume*) is achieved at N_T = 5.

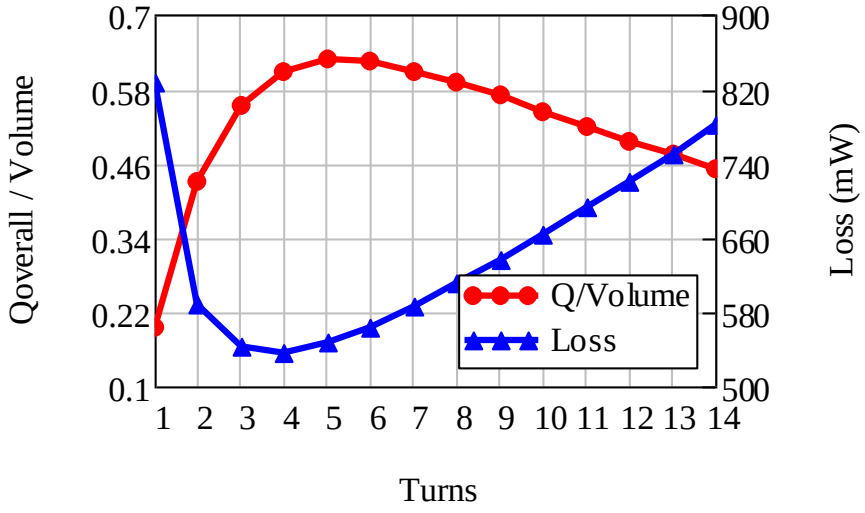

Fig. B.5 Calculated overall Q-factor per volume and loss of a 90 nH inductor.

Appendix C. PCB Spiral Inductor Design

The basic structure of a double layer PCB spiral inductor is shown in Fig. C.1 with dimensions designations.

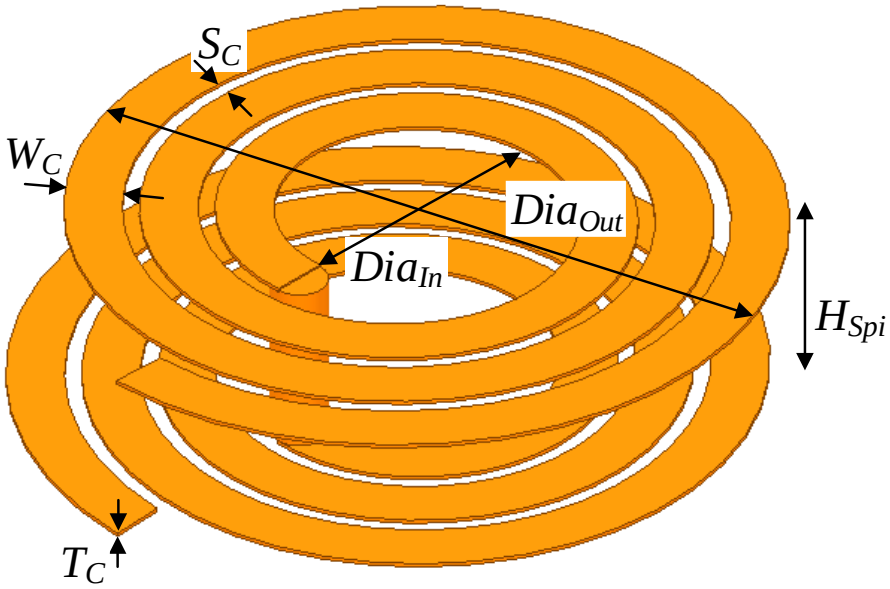

Fig. C.1 PCB spiral inductor structure.

where W_C is the conductor width, S_C is the conductors spacing, Dia_{In} and Dia_{Out} are the spiral inner and outer diameter respectively, H_{Spi} is the inductor's overall height, and T_C is the conductor thickness.

C.1 Inductance

The spiral inductor inductance can be calculated as in [90] but adjusted for double layer configuration:

$$L_S = 0.5\mu_0(1 + k_f)N_{Layers}{N_T}^2 Dia_{Avg}\left(ln\left(\frac{2.46}{P}\right) + 0.2P^2\right) \quad \text{(C.1)}$$

where μ_0 is the air permeability $\mu_0 = 4\pi 10^{-7}$, N_T is the number of turns, N_{Layers} is the number of the PCB series-connected layers, k_f is the coupling factor between layers, Dia_{Avg} is the average spiral diameter $Dia_{Avg} = 0.5(Dia_{Out} + Dia_{In})$, and P is the spiral fill factor calculated as follows:

$$P = \frac{Dia_{Out} - Dia_{In}}{Dia_{Out} + Dia_{In}} = \frac{1 - Dia_{Ratio}}{1 + Dia_{Ratio}} \tag{C.2}$$

where $Dia_{Ratio} = Dia_{In} / Dia_{Out}$ which is the inner to outer diameter ratio.

Then the spiral inductor inductance can be analyzed as a function of Dia_{Ratio}, which leads to a clear design procedure as Dia_{Ratio} ranges from 0 to 1 only.

C.2 PCB manufacturing related parameters

D_{Via}, S_C, T_C and H_{Spi} are predetermined according to the PCB manufacturer capabilities i.e., detailed in Appendix B, and N_{Layers} is equal to the number of the PCB board layers.

The conductor width W_C is calculated as detailed in Appendix B.

C.3 Outer diameter calculation

With the previously mentioned assumptions for the PCB spiral inductor, L_S can be reduced to a function of (Dia_{Out}, Dia_{Ratio}). Then (B.1) can be solved for Dia_{Out} as a function of Dia_{Ratio}, which gives three solutions but only one solution is true i.e.:

$$Dia_{Out} = \frac{\sqrt[3]{\sqrt{{b_1}^2 + 4{b_2}^3} + b_1}}{3\sqrt[3]{2}a_3} - \frac{3\sqrt[3]{2}b_2}{3a_3\sqrt[3]{\sqrt{{b_1}^2 + 4{b_2}^3} + b_1}} - \frac{a_2}{3a_3} \tag{C.3}$$

where

$$a_0 = \frac{-16L_s(W_C + S_C)^2}{N_{Layers}(1 + k_f)\mu_0(1 + Dia_{Ratio})\left[ln\left(\frac{2.46}{\frac{1 - Dia_{Ratio}}{1 + Dia_{Ratio}}}\right) + 0.2\left(\frac{1 - Dia_{Ratio}}{1 + Dia_{Ratio}}\right)^2\right]} \tag{C.4}$$

$$a_1 = (1.5W_C - 0.5S_C)^2 \tag{C.5}$$

$$a_2 = 2(1 - Dia_{Ratio})(1.5W_C - 0.5S_C) \tag{C.6}$$

$$a_3 = (1 - Dia_{Ratio})^2 \tag{C.7}$$

$$b_1 = -27a_0{a_3}^2 + 9a_1a_2a_3 - 2{a_2}^3 \tag{C.8}$$

$$b_2 = 3a_1a_3 - {a_2}^2 \tag{C.9}$$

For a double layer spiral, k_f was found around 0.27 using FEA. For practical PCB layout, the dimensions in mm are rounded up for one decimal place, then L_S is recalculated to make sure that selected dimensions are correct. Designs of a 90 nH inductor are presented in Fig. C.2 showing the effect of the Dia_{Ratio} on D_{Out} while maintaining L_S value.

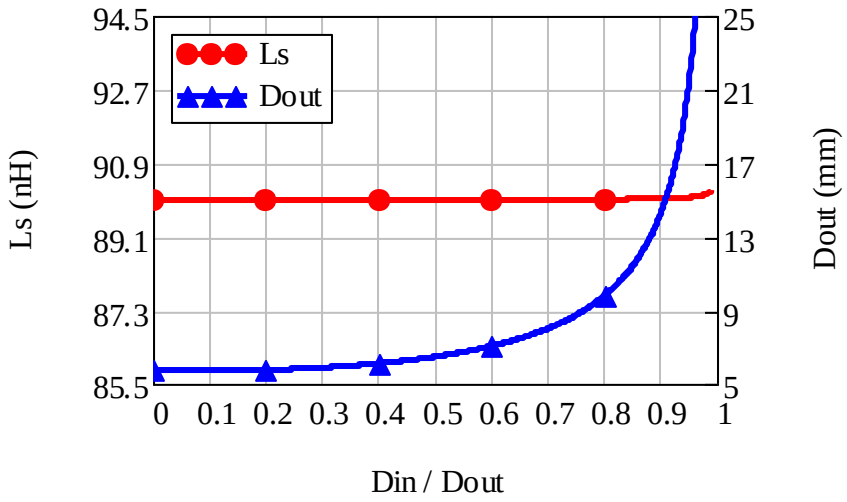

Fig. C.2 L_S and D_{Out} of 90 nH double layer spiral inductor.

C.4 Other design parameters

The remaining design parameters are calculated as follows:

Number of turns

$$N_T = \frac{Dia_{Out}(1 - Dia_{Ratio}) + 2S_C - 0.5(W_C + S_C)}{2(W_C + S_C)} \tag{C.10}$$

Starting inner radius

$$R_{In} = 0.5Dia_{Out} - 0.5(W_C + S_C) - N_T W_C - (N_T - 1)S_C \tag{C.11}$$

Inner diameter

$$Dia_{In} = 2R_{In} + 0.5(W_C + S_C) \tag{C.12}$$

Footprint overall area

$$Area = {Dia_{Out}}^2 \tag{C.13}$$

For a spiral inductor on a double layer PCB with 1.6 mm height, the effect of Dia_{Ratio} on the required number of turns and the resulting inductor volume is shown in Fig. C.3.

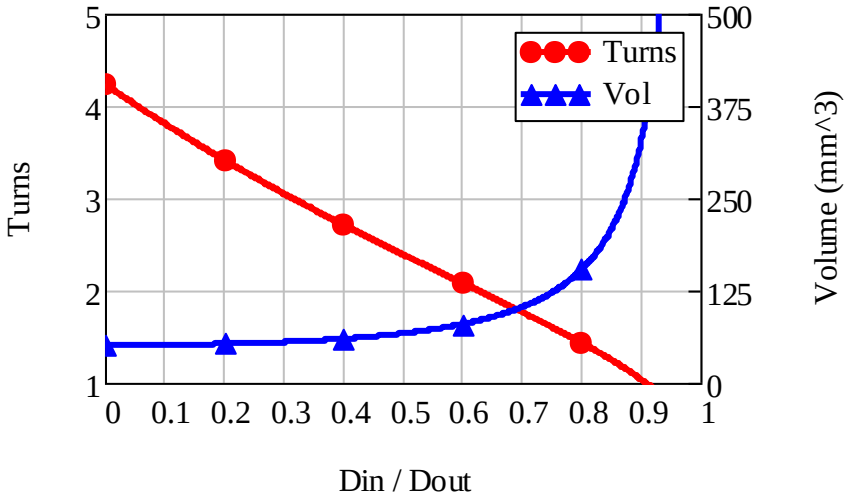

Fig. C.3 Designs of 90 nH inductor.

C.5 DC resistance

DC resistance of the spiral inductor can be calculated as:

$$R_{DC} = \frac{\rho N_{Layers} \ell_{Spiral}}{W_C T_C} \tag{C.14}$$

where ℓ_{Spiral} is the spiral inductor length per layer and ρ is the copper conductivity 1.72x10^{-8} Ωm. ℓ_{Spiral} is derived and is calculated as:

$$\ell_{Spiral} = \int_0^{2\pi N_T} \sqrt{\left(R_{In} + \frac{W_C}{2} + \frac{W_C + S_C}{2\pi}\theta\right)^2 + \left(\frac{W_C + S_C}{2\pi}\right)^2}\, d\theta \tag{C.15}$$

C.6 Inductor power loss and overall Q-factor

Calculation of the total inductor power loss is the overall Q-factor are presented in Appendix B. For an optimum choice of Dia_{Ratio} and the number of turns, $Q_{Overall}$ per inductor volume is considered for benchmarking and design point selection where the maximum ($Q_{Overall}$ / *Volume*) value is close to the design point.

C.7 PCB spiral design example

The previously detailed design procedure is applied for requirements of L_S = 90 nH at ΔT = 50 ^{O}C and DC current rating of 3A. The inductor ($Q_{Overall}$ / *Volume*) and loss are presented in Fig. C.4 for the 90 nH inductor example, and it shows that the ($Q_{Overall}$ / *Volume*) from Dia_{Ratio} = 0 to 0.4 approximately is close to the maximum achieved value, however, inductor loss is minimum at Dia_{Ratio} = 0.5. Hence, the design point at N_T = 3 and Dia_{Ratio} = 0.3155 is selected as a balanced point.

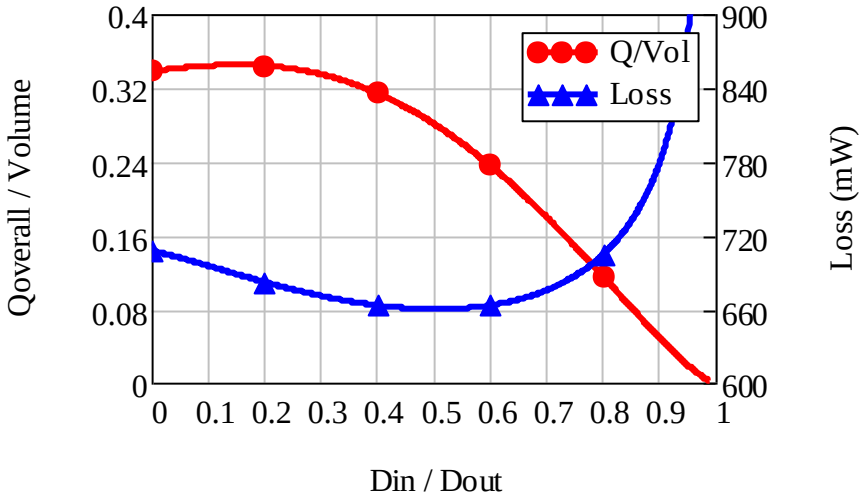

Fig. C.4 Calculated overall Q-factor per volume and loss of a 90 nH inductor.

Appendix D. FPGA Project for Pulse Generation

The gate drivers in the testing prototypes were driven using an FPGA development board which was used to generate the Pulse Width Modulation (PWM) signal for two phases with a 180^{O} phase difference. The FPGA project top-level block schematic and detailed schematic are shown in Fig. D.1 and Fig. D.2 respectively. The project inputs and outputs are defined as follows:

- Inputs
  - clk_sys: clock signal from the onboard oscillator.
  - Duty_inc: button input for duty cycle increment.
  - Duty_rst: button input for duty cycle decrement.
  - enable1: enable switch for the PWM signal of phase 1.
  - enable2: enable switch for the PWM signal of phase 2.
- Outputs
  - PWM_phase1: PWM signal for phase 1.
  - PWM_phase2: PWM signal for phase 2.

The FPGA program is written in VHDL language and its code is presented in this section.

```
----------------------------------------------------------------------------
----------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.numeric_std.all;

library unisim;
use unisim.vcomponents.all;

entity PulseGen_vhdl_src is

     generic(
            constant Bit_res : integer := 4;
            Count_max: std_logic_vector(4 downto 0):= "11111";
            Count_max_2: std_logic_vector(4 downto 0):= "01111";
            Dmin: std_logic_vector(4 downto 0):= "00010";
            Dmax: std_logic_vector(4 downto 0):= "11100");
     Port (
            enable1,enable2 : in  STD_LOGIC;
            clk_sys : in  STD_LOGIC;
          Duty_inc : in  STD_LOGIC;
            Duty_rst : in  STD_LOGIC;
```

```
            PWM_phase1 : out  STD_LOGIC;
            PWM_phase2 : out  STD_LOGIC);
end PulseGen_vhdl_src;

architecture Behavioral of PulseGen_vhdl_src is

    signal clk_1: std_logic;
    signal PWM_tmp: std_logic;
    signal DutyCycle: std_logic_vector(Bit_res downto 0);
    signal Duty2: std_logic_vector(Bit_res+1 downto 0);
    signal count1: std_logic_vector(Bit_res downto 0);
    signal count2: std_logic_vector(Bit_res+2 downto 0);

    component myClock1
    port
     (-- Clock in ports
      CLK_IN1           : in     std_logic;
      -- Clock out ports
      CLK_OUT1          : out    std_logic
     );
    end component;

begin
-----------------------------------------------------------------------
    myClock1_instance : myClock1
      port map
        (-- Clock in ports
         CLK_IN1 => clk_sys,
         -- Clock out ports
         CLK_OUT1 => clk_1
         );
-----------------------------------------------------------------------
    process(Duty_inc,Duty_rst,DutyCycle)
    begin
            if((Duty_rst ='1') or (DutyCycle < Dmin) or (DutyCycle >
Dmax)) then
                DutyCycle <= Dmin;
            elsif ( rising_edge(Duty_inc)) then
                DutyCycle <= DutyCycle + '1';
            end if;
            Duty2 <= ('0'& DutyCycle) +('0'& DutyCycle);
    end process;
-----------------------------------------------------------------------
    process(clk_1,Duty_rst) -- Counting
    begin
        if(rising_edge(clk_1)) then
            if (count1 < Count_max) and (Duty_rst /='1') then
                count1 <= count1 + 1;
                count2 <= ('0'&'0'& count1) + ('0'&'0'& count1)+"10";
            else
                count1 <=(others => '0'); --set all bits to 0
                count2 <=(others => '0');
            end if;
        end if;
    end process;
-----------------------------------------------------------------------
    process(clk_1) -- PWM_1 ouput
    begin
        if(rising_edge(clk_1)) then
            if (Duty2 <= Count_max) then --D<=0.5and
```

```
                if (count1 <= DutyCycle) then
                    PWM_phase1 <= enable1 and '1';
                    PWM_phase2 <= enable2 and '0';
                else
                    if (count2 > Count_max) and (count2 <
('0'&Count_max) + Duty2+"10") then
                        PWM_phase1 <= enable1 and '0';
                        PWM_phase2 <= enable2 and '1';
                    else
                        PWM_phase1 <= enable1 and '0';
                        PWM_phase2 <= enable2 and '0';
                    end if;
                end if;

            else --D>0.5

                if (count1 > DutyCycle) then
                    PWM_phase1 <= enable1 and '0';
                    PWM_phase2 <= enable2 and '1';
                else
                    if (('0'&count2)+('0'&'0'&'0'&Count_max) > Duty2)
and (('0'&count2)+('0'&'0'&'0'&Count_max) <
('0'&'0'&Count_max)+('0'&'0'&Count_max)) then
                        PWM_phase1 <= enable1 and '1';
                        PWM_phase2 <= enable2 and '0';
                    else
                        PWM_phase1 <= enable1 and '1';
                        PWM_phase2 <= enable2 and '1';
                    end if;
                end if;

            end if;
        end if;
    end process;

end Behavioral;
----------------------------------------------------------------------------
----------------------------------------------------------------------------
```

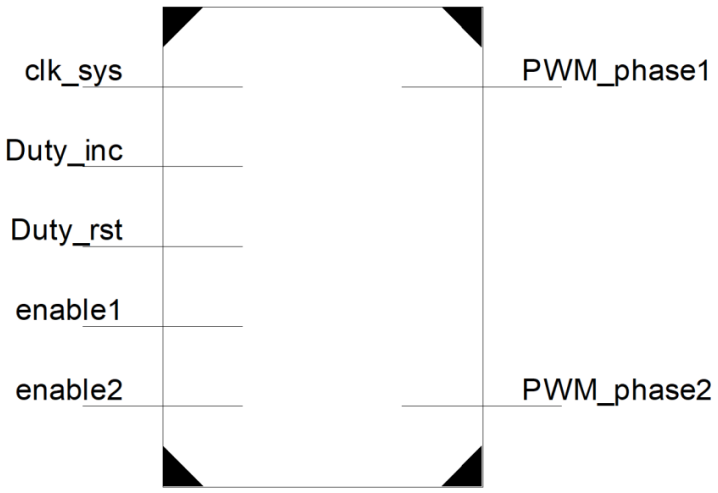

Fig. D.1 FPGA project top level block schematic.

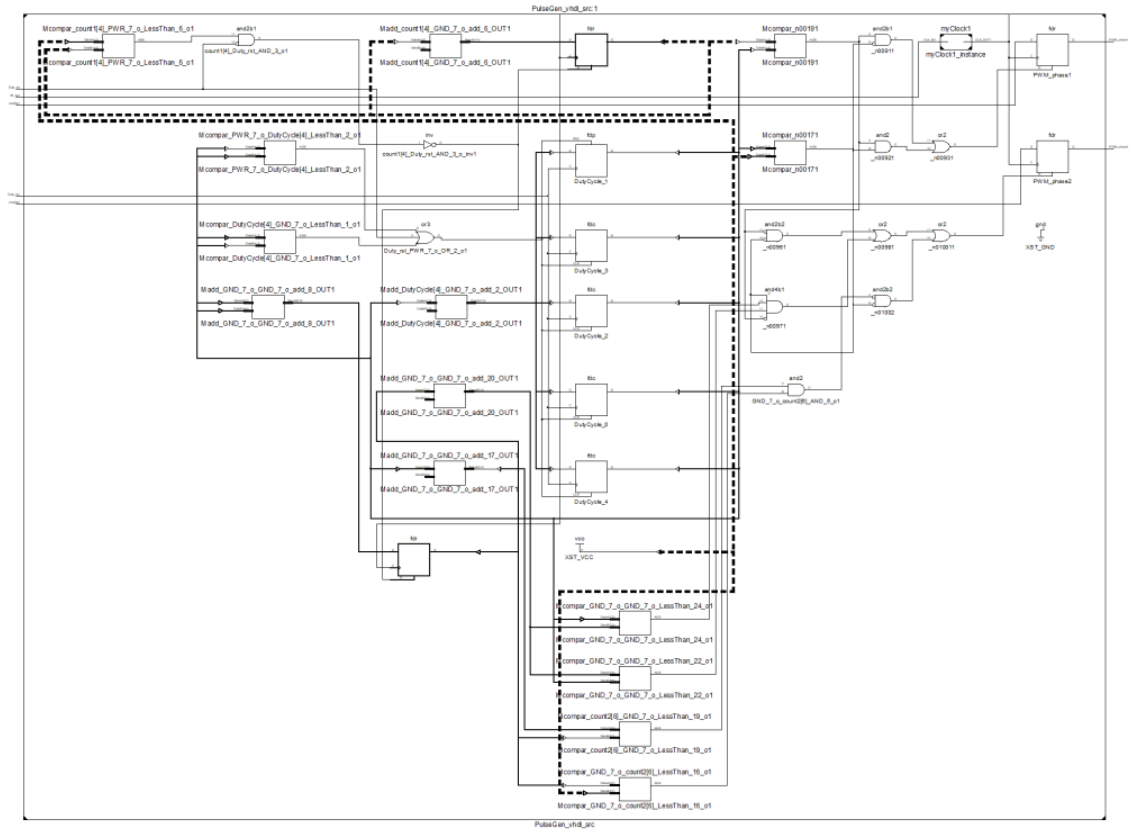

Fig. D.2 FPGA project detailed schematic.