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A Dual Image Processing Pipeline Camera with CE Applications

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Abstract—The implementation of a dual image processing pipeline camera on a state-of-art FPGA system is described. This camera can simultaneously acquire dual images of a scene and process, analyze and merge both images to enable a range of real-time image enhancement algorithms to be explored. Several examples of image enhancement algorithms implemented on the prototype camera are described.

I. INTRODUCTION

In a state-of-art digital camera the final picture is very different from the initial raw image captured by the CMOS sensor. Typically this raw data will have been de-mosaiced from Bayer to RGB or YCC and subsequently its white and color balance will be adjusted. Additional post-filtering is often applied to compensate for flash-eye defects or the chromatic aberrations or purple-fringing effects caused by a low-cost lens. Many cameras also track faces and adjust the final acquisition to optimize skin color and facial features.

All of this image-processing magic that consumers now take for granted occurs within what is known as the *image processing pipeline* (IPP) of the camera. Typically much of the heavy lifting is performed by a dedicated image processing CPU which often features parallelized hardware extensions to speed up common operations such as demosaicking, DCT transformation, color segmentation and creation of an integral image.

As we reach the limits of conventional image acquisition hardware and camera systems it becomes increasingly evident that two pictures are better than one. For example, advanced techniques of red-eye removal use a reference image captured without flash to help localize genuine red-eyes [13]; a blurred image can be corrected by combining with an underexposed sharp image of the same scene [5], [6]; back-lit scenes can be uniformly exposed by combining images with different exposure levels [ref3] and the perceptual depth of a scene can be significantly enhanced by combining images with differing depths of focus [ref4].

However a drawback with all of these techniques is that the two images must be captured sequentially and some misalignment and camera motion between the two capture events is unavoidable. A further drawback is that the two images to be combined must be either in RAW format, or alternatively processed by the IPP prior to combination. As has been pointed out by some authors [2], the order in which various operations of the IPP are applied can have significant effects on the final image.

This leads us to the key motivation for the work presented in this paper. Ideally we should be able to capture two images of the same scene *at the same time*, thus avoiding the issues introduced by inter-scene motion and image alignment. This requires a dual imaging system. Furthermore, many of the algorithms mentioned above require the two images to be combined at the pixel level – typically via a fixed size kernel, or alternatively via an adaptive FIR filter. Thus it is desirable not only to have a dual acquisition system, but also to have a flexible dual-IPP which can implement the various functions of a conventional IPP independently on each image and also implement the real-time pixel combining of the two input images. Such a prototype device allows us to experiment practically with different two-picture enhancement algorithms and, most importantly, to adapt the order in which IPP functions and image combination filters are applied.



Fig 1: A Typical Image Processing Pipeline

Modern electronic systems based on FPGA devices are sufficiently powerful enough to implement a dual-IPP which allows us to capture synchronized images of the same original scene [1, 11]. This further enables us to test and verify various image processing algorithms and develop new methods to process and enhance dual-images.

II. THE DUAL PIPELINE CAMERA

A. Hardware Overview

The general hardware architecture of the dual-pipeline camera can be seen in figure 2. This design is implemented using an ML405 development board with a Virtex 4TM FPGA device. Two 1 Megapixel image sensors are employed to provide a dual acquisition system. In our initial prototype we use two independent imaging elements, although certain applications may require a common primary optical path split between the two image sensors.

The various components of the IPP chain are implemented in the FPGA. A PLB (Processor Local Bus) is used to provide bulk data transfer between these image processing components and the DDR SDRAM. These individual hardware modules are controlled by an internal PowerPC RISC microprocessor which is available with this famile of FPGAs. Control operations are managed via a separate DCR (Data Control Register) bus. An I2C controller is also implemented on board the FPGA and this enables control of the dual image sensors either simultaneously or independently.



Fig.2. Internal FPGA Architecture

The sensors used are 1/3 inch SXGA CMOS sensors with an active zone of 1280x1024 pixels. They are programmable through an I2C interface. These sensors are clocked at a frequency of 25 Mhz. They were selected because of the small size, low cost and the imaging capabilities are ideally matched to the memory size and processing bandwidth of the FPGA.



Fig. 3. Dual-IPP Camera Prototype

III. A SUMMARY OF TWO-IMAGE ALGORITHMS

Here we provide a brief overview of some of the image enhancement algorithms which may be optimized on our dual-IPP camera.

A. Flash/No-flash Photography

One image enhancement applications which can benefit from our dual-IPP camera is that of foreground extraction from images [3]. This flash cut technique handles the segmentation problem by fusing flash, motion and color cues. The information from flash is exploited globally using histogram analysis and locally with the help of background motion information. Foreground extraction enables various enhancements of the final image including application of the Bokeh effect to the background image [14].

A second image enhancement involves the removal of shadows from images [4]. These authors show that first applying a "spectrally sharpened" color space to an image, and then focusing on the difference in a log domain of the flash minus the ambient image, gives a very simple feature space consisting of two components. This space provides excellent separation of the shadow and nonshadow areas.

B. Complimentary Image Exposures

This second category of dual-image algorithm involves the merging of two images with significantly different exposure characteristics. In one set of applications the problem of motion blur in images can be addressed by combining a sharp underexposed image with a second, normally exposed but blurred image. The first image preserves the scene detail and structure while the colorimetric data is captured in the second, blurred image.

Several authors have realized this technique [5], [6]. We remark that the authors of [6] have provided a pixel-level adaptive filter which can be directly implemented in FPGA hardware.

C. Depth Map Generation

Another potential application is that of depth map generation. This enables additional image data which can be used to enhance 2D image, or even generate pseudo 3D images on-the-fly.

There are two distinct approaches. The first is to employ the information from a pair of synchronized stereo images as presented in [7, 8]. The point-by-point matching between the two images can be used to generate a depth map. This matching can be done as a one-dimensional search given the stereo images are callibrated.

A second method of depth map generation is the depth from defocus (DfD) method s presented in [9, 10]. The concept of depth from defocus involves calculating distances to points in an observed scene by modeling the effect that the camera's focal parameters have on images acquired with a small depth of field. The ability of the dual-IPP camera to simulanenously capture two images with different focal lengths offers advantages over conventional single-camera DfD techniques.

IV. CONCLUSIONS

The dual-IPP camera system offers an excellent platform on which to explore a range of next-generation imaging algorithms. A number of examples will be presented at our conference presentation and a full technical paper will be submitted to the CE Transactions giving details of some of our initial experimental results with several of these dualimage enhancement techniques.

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